(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 339 065 A2

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
27.08.2003 Bulletin 2003/35

(51) Int Cl.[7]: **G11C 11/16**

(21) Application number: **03003242.9**

(22) Date of filing: **21.02.2003**

(84) Designated Contracting States:
AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IT LI LU MC NL PT SE SI SK TR
Designated Extension States:
AL LT LV MK RO

(30) Priority: **22.02.2002 JP 2002046964**

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(54) Magnetic random access memory

(57) A read block (BK11) is formed from a plurality of MTJ elements (12) arranged in the horizontal direction. One terminal of each MTJ element (12) in the read block (BK11) is commonly connected. The connection point is directly connected to a read word line (RWL1) without intervening a select switch. The other terminal of each MTJ element (12) is individually connected to a read bit line (RBL1,..., RBL4)/write word line (WWL1,..., WWL4). The read bit line (RBL1,..., RBL4)/write word line (WWL1,..., WWL4) is connected to a common data line (30) through a row select switch (RSW2). The common data line (30) is connected to a read circuit (29B).

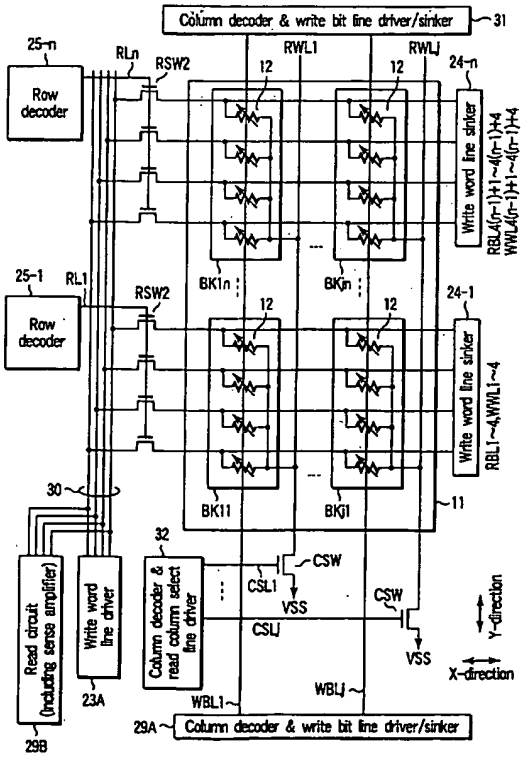

FIG. 1

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Description

[0001] The present invention relates to a magnetic random access memory (MRAM) which utilizes a magnetoresistive effect.

[0002] In recent years, many memories which store data by new principles have been proposed. One of them is a magnetic random access memory which utilizies the tunneling magnetoresistive (to be referred to as TMR hereinafter) effect.

[0003] As a proposal for a magnetic random access memory, for example, Roy Scheuerlein et al, "A 10ns Read and Write Non-Volatile Memory Array Using a Magnetic Tunnel Junction and FET Switch in each Cell", ISSCC2000 Technical Digest, p. 128 is known.

[0004] A magnetic random access memory stores "1"- and "0"-data using MTJ (Magnetic Tunnel Junction) elements. As the basic structure of a MTJ element, an insulating layer (tunneling barrier) is sandwiched between two magnetic layers (ferromagnetic layers). However, various kinds of MTJ element structures have been proposed to, e.g., optimize the MR (MagnetoResistive) ratio.

[0005] Data stored in the MTJ element is determined on the basis of whether the magnetizing states of the two magnetic layers are parallel or antiparallel. "Parallel" means that the two magnetic layers have the same magnetizing direction. "Antiparallel" means that the two magnetic layers have opposite magnetizing directions.

[0006] Normally, one (fixed layer) of the two magnetic layers has an antiferromagnetic layer. The antiferromagnetic layer serves as a member for fixing the magnetizing direction of the fixed layer. In fact, data ("1" or "0") stored in the MTJ element is determined by the magnetizing direction of the other (free layer) of the two magnetic layers.

[0007] When the magnetizing states in the MTJ element are parallel, the tunneling resistance of the insulating layer (tunneling barrier) sandwiched between the two magnetic layers of the MTJ element is minimized. For example, this state is defined as a "1"-state. When the magnetizing states in the MTJ element are antiparallel, the tunneling resistance of the insulating layer (tunneling barrier) sandwiched between the two magnetic layers of the MTJ element is maximized. For example, this state is defined as a "0"-state.

[0008] Currently, various kinds of cell array structures have been examined for a magnetic random access memory from the viewpoint of increasing the memory capacity or stabilizing write/read operation.

[0009] For example, currently, a cell array structure in which one memory cell is formed from one MOS transistor and one MTJ element is known. Additionally, a magnetic random access memory which has such a cell array structure and stores 1-bit data using two memory cell arrays so as to realize stable read operation is also known.

[0010] However, in these magnetic random access memories, it is difficult to increase the memory capacity. This is because one MOS transistor corresponds to one MTJ element in these cell array structures.

[0011] As a magnetic random access memory which needs no MOS transistors in the memory cell array, a cross-point cell array structure is conventionally known. A cross-point cell array structure has a simple structure with an MTJ element being arranged at the interconnection of a word line and a bit line. As a characteristic feature, no select transistor is arranged in the memory cell array.

[0012] According to the cross-point cell array structure, the memory cell size can be reduced because no select MOS transistors are used. As a consequence, the memory capacity can be increased.

[0013] For example, when the minimum size of design rule is defined as "F", the size of a memory cell formed from a select MOS transistor and MTJ element is $8F^2$. However, a memory cell including only an MTJ element is $4F^2$. That is, the memory cell including only an MTJ element can realize a cell size about 1/2 that of the memory cell formed from a select MOS transistor and MTJ element.

[0014] However, when a magnetic random access memory is formed by employing a cross-point cell array structure, there is posed a problem of breakdown of the insulting layer (tunneling barrier layer) of a TMR (MTJ) element in write operation.

[0015] More specifically, in the cross-point cell array structure, an MTJ element is arranged at the intersection of a word line and a bit line while being in contact with them. Write currents having the same value are supplied to the word line and bit line (the directions of the write currents supplied to the word line and bit line change in accordance with the data value) to generate a magnetic field. The direction of magnetization of the MTJ element arranged between the word line and the bit line is thus determined.

[0016] The word line and bit line have interconnection resistances. The value of the interconnection resistance across the word line and bit line increases as they become long. That is, when the write current is flowing, the potential at a position close to the driver of the word line or bit line is higher than that at a position close to the sinker of the word line or bit line.

[0017] Hence, in write operation, a potential difference may be generated across the MTJ element in accordance with its position. This potential difference may cause voltage stress on the tunneling barrier layer of the MTJ element and then dielectric breakdown of the tunneling barrier layer.

[0018] This problem will be described in detail.

[0019] An MTJ element (worst case) which is arranged at a position closest to a word line driver WD (farthest from a word line sinker WS) and closest to a bit line sinker BS (farthest from a bit line driver BD), as shown in FIG. 107, will be examined.

[0020] The potential at the word-line-side end portion

of the MTJ element is, e.g., Vp because the end portion is in contact with the word line at a position closest to the word line driver WD. On the other hand, the potential at the bit-line-side end portion of the MTJ element is, e. g., Vp-α because the end portion is in contact with the bit line at a position farthest from the bit line driver BD, and a voltage drop occurs due to an interconnection resistance r of the bit line.

[0021] That is, the potential of the bit-line-side end portion of the MTJ element is lower than that of the word-line-side end portion by α. As a result, the potential difference α is generated across the MTJ element arranged at the closest to the word line driver WD and bit line sinker BS.

[0022] Assume that dielectric breakdown of the tunneling barrier layer is caused by an electric field more than 10 [MV/cm] at a very high probability.

[0023] When the sheet resistance of the word line and bit line is 100 [mΩ], and the size of the memory cell array is 1750 (1.75 kilo) cells × 1750 (1.75 kilo) cells, the interconnection resistance r from one end to the other end of the word line or bit line is as follows.

[0024] In the cross-point cell array structure, memory cells are arranged along the word lines and bit lines from one end to the other end of each of them. When a memory cell has a minimum process size (design rule) in the direction in which the word line or bit line runs, the pitch between the memory cells in that direction is also set to the minimum process size (pitch).

[0025] That is, the length of a word line or bit line corresponds to an array of 1750 × 2 memory cells. Hence, the interconnection resistance r from one end to the other end of the word line or bit line is 350 [Ω] (when the memory cell array becomes large, the word lines and bit lines become long, and the interconnection resistance r increases).

[0026] When the interconnection resistance r is 350 [Ω], and a write current Ip is 2 [mA], a potential difference of 0.7 (= 0.002 × 350) [V] is generated across each of the word lines and bit lines.

[0027] When the thickness of the tunneling barrier layer of the MTJ element (when the MTJ element has a plurality of tunneling barrier layers, the total thickness of the tunneling barrier layers) is 0.7 [nm], and the potential difference across the MTJ element is 0.7 [V], an electric field of 10 [MV/cm] is generated in the MTJ element.

[0028] To avoid dielectric breakdown of the tunneling barrier layer under the above conditions, the size of one memory cell array surrounded by the word line driver/sinker and bit line driver/sinker must be set to 1.75 kilo × 1.75 kilo or less.

[0029] As described above, in the cross-point cell array structure, when dielectric breakdown of the tunneling barrier layer of the MTJ element in write operation is taken into consideration, the upper limit of the memory cell array size is determined. Hence, the degree of integration of MTJ elements cannot be sufficiently increased.

[0030] In addition, the write current Ip does not always flow to the word line or bit line. The write current Ip is supplied to the word line or bit line only in the write operation. That is, the potential at a position closest to the word line or bit line sometimes exceeds Vp due to overshoot phenomenon.

[0031] In consideration of this overshoot phenomenon, an electric field more than 10 [MV/cm] may be generated in the MTJ element under the above conditions.

[0032] Assume that the sheet resistance of the word line and bit line, the write current Ip, and the thickness of the tunneling barrier layer are constant. In this case, to avoid probable generation of an electric field more than 10 [MV/cm] in the MTJ element at a high possibility, the memory cell array size must be further reduced to decrease the voltage drop amount due to the interconnection resistance r of the word line or bit line.

[0033] For example, overshoot of the potential on the word line or bit line will be examined under the above conditions. The upper limit size of one memory cell array must be decreased from 3 mega (= 1.75 kilo × 1.75 kilo) to 1.5 mega.

[0034] A clamp circuit which clamps the potential of the word line or bit line may be newly arranged as a peripheral circuit of the memory cell array to prevent the overshoot/undershoot phenomenon.

[0035] In this case, however, the size of the peripheral circuits increases as the clamp circuit is added. In addition, the clamp circuit has a function of suppressing abrupt increase/decrease in potential of the word line or bit line. For this reason, changing the potential of the word line or bit line to Vp takes a long time, resulting in a decrease in write speed.

[0036] A magnetic random access memory according to a first example of the present invention comprises a memory cell array having memory cells which utilizes a magnetoresistive effect, a first functional line which runs in a first direction in the memory cell array and is commonly connected to one terminal of each of the memory cells, second functional lines which are arranged in correspondence with the memory cells and run in a second direction perpendicular to the first direction in the memory cell array, and a third functional line which is separated from the memory cells and shared by the memory cells. The other terminal of each of the memory cells is independently connected to one of the second functional lines, and one terminal of each of the memory cells is directly connected to the first functional line.

[0037] A magnetic random access memory according to a second example of the present invention comprises a memory cell array having a memory cell which utilizes a magnetoresistive effect, a first functional line which runs in a first direction in the memory cell array and is connected to one terminal of the memory cell, a second functional line which runs in a second direction perpendicular to the first direction in the memory cell array and is connected to the other terminal of the memory cell,

and a third functional line which is separated from the memory cell and generates a magnetic field to write data in the memory cell. One terminal of the memory cell is directly connected to the first functional line, and the other terminal of the memory cell is directly connected to the second functional line.

[0038] A read method of a magnetic random access memory according to a third example of the present invention comprises fixing all the second functional lines to a first potential, setting the first functional line to a second potential different from the second potential, individually supplying a read current to the memory cells, and reading out data from the memory cells on the basis of a value of the read current.

[0039] A write method of a magnetic random access memory according to a fourth example of the present invention comprises supplying a first write current flowing in one direction to one of the second functional lines, supplying a second write current having a direction depending on write data to the third functional line, and writing the write data in one of the memory cells using a magnetic field generated by the first and second write currents.

[0040] A write method of a magnetic random access memory according to a fifth example of the present invention comprises supplying a first write current having a direction depending on write data to one of the second functional lines, supplying a second write current flowing in one direction to the third functional line, and writing the write data in one of the memory cells using a magnetic field generated by the first and second write currents.

[0041] A manufacturing method of a magnetic random access memory according to a sixth example of the present invention comprises the first step of forming a gate electrode of a MOS transistor in a peripheral circuit region and simultaneously forming, in a memory cell array region, dummy interconnections equidistantly, periodically, or in a layout uniform as a whole, the second step of forming a first interlayer dielectric film which covers the MOS transistor and dummy interconnections, the third step of forming a memory cell having a magnetoresistive effect in a surface region of the first interlayer dielectric film in the memory cell array region, and the fourth step of forming a second interlayer dielectric film which covers the memory cell.

[0042] This summary of the invention does not necessarily describe all necessary features so that the invention may also be a sub-combination of these described features.

[0043] The invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

FIG. 1 is a circuit diagram showing a magnetic random access memory according to Structural Example 1 of the present invention;
FIG. 2 is a sectional view showing Device Structure 1 according to Structural Example 1;
FIG. 3 is a plan view showing Device Structure 1 according to Structural Example 1;
FIG. 4 is a sectional view showing Device Structure 2 according to Structural Example 1;
FIG. 5 is a plan view showing Device Structure 2 according to Structural Example 1;
FIG. 6 is a plan view showing Device Structure 2 according to Structural Example 1;
FIG. 7 is a plan view showing Device Structure 2 according to Structural Example 1;
FIG. 8 is a sectional view showing Device Structure 3 according to Structural Example 1;
FIG. 9 is a plan view showing Device Structure 3 according to Structural Example 1;
FIG. 10 is a plan view showing Device Structure 3 according to Structural Example 1;
FIG. 11 is a plan view showing Device Structure 3 according to Structural Example 1;
FIG. 12 is a plan view showing Device Structure 3 according to Structural Example 1;
FIG. 13 is a view showing the outline of a magnetic random access memory according to Structural Example 2 of the present invention;
FIG. 14 is a sectional view showing Device Structure 1 according to Structural Example 2;
FIG. 15 is a sectional view showing Device Structure 2 according to Structural Example 2;
FIG. 16 is a circuit diagram showing a magnetic random access memory according to Structural Example 3 of the present invention;
FIG. 17 is a circuit diagram showing the magnetic random access memory according to Structural Example 3 of the present invention;
FIG. 18 is a sectional view showing a device structure according to Structural Example 3;
FIG. 19 is a plan view showing a device structure according to Structural Example 3;
FIG. 20 is a plan view showing a device structure according to Structural Example 3;
FIG. 21 is a plan view showing a device structure according to Structural Example 3;
FIG. 22 is a plan view showing a device structure according to Structural Example 3;
FIG. 23 is a plan view showing a device structure according to Structural Example 3;
FIG. 24 is a circuit diagram showing a magnetic random access memory according to Structural Example 4 of the present invention;
FIG. 25 is a circuit diagram showing the magnetic random access memory according to Structural Example 4 of the present invention;
FIG. 26 is a sectional view showing a device structure according to Structural Example 4;
FIG. 27 is a plan view showing a device structure according to Structural Example 4;
FIG. 28 is a plan view showing a device structure according to Structural Example 4;

FIG. 29 is a plan view showing a device structure according to Structural Example 4;
FIG. 30 is a plan view showing a device structure according to Structural Example 4;
FIG. 31 is a plan view showing a device structure according to Structural Example 4;
FIG. 32 is a plan view showing a device structure according to Structural Example 4;
FIG. 33 is a plan view showing a device structure according to Structural Example 4;
FIG. 34 is a circuit diagram showing a magnetic random access memory according to Structural Example 5 of the present invention;
FIG. 35 is a circuit diagram showing the magnetic random access memory according to Structural Example 5 of the present invention;
FIG. 36 is a sectional view showing a device structure according to Structural Example 5;
FIG. 37 is a plan view showing a device structure according to Structural Example 5;
FIG. 38 is a plan view showing a device structure according to Structural Example 5;
FIG. 39 is a plan view showing a device structure according to Structural Example 5;
FIG. 40 is a plan view showing a device structure according to Structural Example 5;
FIG. 41 is a plan view showing a device structure according to Structural Example 5;
FIG. 42 is a plan view showing a device structure according to Structural Example 5;
FIG. 43 is a plan view showing a device structure according to Structural Example 5;
FIG. 44 is a circuit diagram showing a magnetic random access memory according to Structural Example 6 of the present invention;
FIG. 45 is a circuit diagram showing the magnetic random access memory according to Structural Example 6 of the present invention;
FIG. 46 is a sectional view showing a device structure according to Structural Example 6;
FIG. 47 is a plan view showing a device structure according to Structural Example 6;
FIG. 48 is a plan view showing a device structure according to Structural Example 6;
FIG. 49 is a plan view showing a device structure according to Structural Example 6;
FIG. 50 is a plan view showing a device structure according to Structural Example 6;
FIG. 51 is a plan view showing a device structure according to Structural Example 6;
FIG. 52 is a plan view showing a device structure according to Structural Example 6;
FIG. 53 is a circuit diagram showing a magnetic random access memory according to Structural Example 7 of the present invention;
FIG. 54 is a sectional view showing a device structure according to Structural Example 7;
FIG. 55 is a plan view showing a device structure according to Structural Example 7;
FIG. 56 is a plan view showing a device structure according to Structural Example 7;
FIG. 57 is a plan view showing a device structure according to Structural Example 7;
FIG. 58 is a circuit diagram showing a magnetic random access memory according to Structural Example 8 of the present invention;
FIG. 59 is a circuit diagram showing a magnetic random access memory according to Structural Example 9 of the present invention;
FIG. 60 is a sectional view showing a device structure according to Structural Example 10;
FIG. 61 is a view showing a structural example of an MTJ element;
FIG. 62 is a view showing a structural example of the MTJ element;
FIG. 63 is a view showing a structural example of the MTJ element;
FIG. 64 is a view showing a circuit example of a write word line driver/sinker;
FIG. 65 is a view showing a circuit example of the write word line driver/sinker;
FIG. 66 is a view showing a circuit example of a row decoder;
FIG. 67 is a view showing a circuit example of a column decoder & read column select line driver;
FIG. 68 is a view showing a circuit example of a write bit line driver/sinker;
FIG. 69 is a view showing a circuit example of a write bit line driver/sinker;
FIG. 70 is a view showing a circuit example of a column decoder & write word line driver/sinker;
FIG. 71 is a view showing a circuit example of a row decoder;
FIG. 72 is a view showing a circuit example of a write word line driver;
FIG. 73 is a view showing a circuit example of a row decoder & read line driver;
FIG. 74 is a circuit diagram showing a magnetic random access memory according to Structural Example 11 of the present invention;
FIG. 75 is a view showing a circuit example of a write bit line driver/sinker of FIG. 74;
FIG. 76 is a view showing a circuit example of a write bit line driver/sinker of FIG. 74;
FIG. 77 is a view showing a circuit example of a read circuit;
FIG. 78 is a view showing a circuit example of a read circuit;
FIG. 79 is a view showing a circuit example of a sense amplifier & bit line bias circuit;
FIG. 80 is a view showing a circuit example of a sense amplifier;
FIG. 81 is a view showing a circuit example of a reference potential generation circuit;
FIG. 82 is a view showing a circuit example of an operational amplifier;

FIG. 83 is a view showing a circuit example of a sense amplifier & bit line bias circuit;
FIG. 84 is a view showing MTJ elements arranged symmetrically with respect to a write line;
FIG. 85 is a view showing MTJ elements arranged symmetrically with respect to a write line;
FIG. 86 is a view showing MTJ elements arranged symmetrically with respect to a write line;
FIG. 87 is a view showing MTJ elements arranged symmetrically with respect to a write line;
FIG. 88 is a view showing MTJ elements arranged symmetrically with respect to a write line;
FIG. 89 is a view showing MTJ elements arranged symmetrically with respect to a write line;
FIG. 90 is a view showing a circuit example of a write bit line driver/sinker;
FIG. 91 is a sectional view showing a device structure to which a manufacturing method according to the example of the present invention is applied;
FIG. 92 is a sectional view showing a step in manufacturing according to the example of the present invention;
FIG. 93 is a sectional view showing a step in manufacturing according to the example of the present invention;
FIG. 94 is a sectional view showing a step in manufacturing according to the example of the present invention;
FIG. 95 is a sectional view showing a step in manufacturing according to the example of the present invention;
FIG. 96 is a sectional view showing a step in manufacturing according to the example of the present invention;
FIG. 97 is a sectional view showing a step in manufacturing according to the example of the present invention;
FIG. 98 is a sectional view showing a step in manufacturing according to the example of the present invention;
FIG. 99 is a sectional view showing a step in manufacturing according to the example of the present invention;
FIG. 100 is a sectional view showing a step in manufacturing according to the example of the present invention;
FIG. 101 is a sectional view showing a step in manufacturing according to the example of the present invention;
FIG. 102 is a sectional view showing a step in manufacturing according to the example of the present invention;
FIG. 103 is a sectional view showing a step in manufacturing according to the example of the present invention;
FIG. 104 is a sectional view showing a step in manufacturing according to the example of the present invention;
FIG. 105 is a sectional view showing a step in manufacturing according to the example of the present invention;
FIG. 106 is a sectional view showing a step in manufacturing according to the example of the present invention;
FIG. 107 is a view showing a problem of a cross-point cell array structure;
FIG. 108 is a circuit diagram showing a magnetic random access memory according to Modification example of Structural Example 8;
FIG. 109 is a circuit diagram showing a magnetic random access memory according to Modification example of Structural Example 8;
FIG. 110 is a circuit diagram showing a magnetic random access memory according to Modification example of Structural Example 8;
FIG. 111 is a circuit diagram showing a magnetic random access memory according to Structural Example 12 of the present invention;
FIG. 112 is a circuit diagram showing a magnetic random access memory according to Structural Example 12 of the present invention;
FIG. 113 is a circuit diagram showing a magnetic random access memory according to Structural Example 12 of the present invention;
FIG. 114 is a circuit diagram showing a magnetic random access memory according to Structural Example 12 of the present invention;
FIG. 115 is a circuit diagram showing a magnetic random access memory according to Structural Example 12 of the present invention;
FIG. 116 is a circuit diagram showing a magnetic random access memory according to Structural Example 12 of the present invention;
FIG. 117 is a circuit diagram showing a magnetic random access memory according to Structural Example 12 of the present invention;
FIG. 118 is a circuit diagram showing a magnetic random access memory according to Structural Example 12 of the present invention;
FIG. 119 is a circuit diagram showing a magnetic random access memory according to Structural Example 12 of the present invention;
FIG. 120 is a circuit diagram showing a magnetic random access memory according to Structural Example 12 of the present invention;
FIG. 121 is a circuit diagram showing a magnetic random access memory according to Structural Example 13 of the present invention;
FIG. 122 is a circuit diagram showing a magnetic random access memory according to Structural Example 13 of the present invention;
FIG. 123 is a circuit diagram showing a magnetic random access memory according to Structural Example 13 of the present invention;
FIG. 124 is a circuit diagram showing a magnetic random access memory according to Structural Ex-

ample 13 of the present invention;
FIG. 125 is a circuit diagram showing a magnetic random access memory according to Structural Example 13 of the present invention;
FIG. 126 is a circuit diagram showing a magnetic random access memory according to Structural Example 13 of the present invention;
FIG. 127 is a circuit diagram showing a magnetic random access memory according to Structural Example 13 of the present invention;
FIG. 128 is a circuit diagram showing a magnetic random access memory according to Structural Example 13 of the present invention;
FIG. 129 is a circuit diagram showing a magnetic random access memory according to Structural Example 13 of the present invention;
FIG. 130 is a circuit diagram showing a magnetic random access memory according to Structural Example 13 of the present invention;
FIG. 131 is a circuit diagram showing a magnetic random access memory according to Structural Example 14 of the present invention; and
FIG. 132 is a circuit diagram showing a magnetic random access memory according to Structural Example 15 of the present invention.

[0044] A magnetic random access memory according to an example of the present invention will be described below in detail with reference to the accompanying drawing.

1. Cell Array Structure

[0045] The cell array structure of the magnetic random access memory according to the example of the present invention will be described first.

[0046] As a characteristic feature of the cell array structure according to the example of the present invention, in a cell array structure in which one terminal of each of a plurality of MTJ elements which form a read block is commonly connected, and the other terminal is independently connected to a read bit line, one terminal of each of the plurality of MTJ elements is directly connected to a read word line without intervening a read select switch.

[0047] That is, no read select switch (e.g., a MOS transistor) is arranged in the read block. Consequently, a memory cell array can be formed from only MTJ elements.

[0048] According to this cell array structure, no switch element is arranged in the memory cell array. Hence, the density of MTJ elements can be increased, and the underlying layer of the MTJ elements can be planarized (the magnetoresistive value and MR ratio can be uniformed). In addition, since one of two write lines is separated from MTJ elements, no potential difference is generated across an MTJ element in write operation, unlike a cross-point cell array structure. Hence, the tunneling barrier layer of the MTJ element is not broken.

(1) Structural Example 1

[0049] In Structural Example 1, one read block is formed from four MTJ elements.

① Circuit Structure

[0050] The circuit structure will be described first.

[0051] FIG. 1 shows the main part of a magnetic random access memory according to Structural Example 1 of the present invention.

[0052] A memory cell array 11 has a plurality of MTJ elements 12 arranged in an array in the X- and Y-directions. For example, j MTJ elements 12 are arranged in the X-direction, and 4 × n MTJ elements 12 are arranged in the Y-direction.

[0053] The four MTJ elements 12 arranged in the Y-direction form one read block BKik (i = 1,..., j, and k = 1,..., n). One row is constructed by j read blocks BKik arranged in the X-direction. The memory cell array 11 has n rows. In addition, one column is constructed by n read blocks BKik arranged in the Y-direction. The memory cell array 11 has j columns.

[0054] One terminal of each of the four MTJ elements 12 in the block BKik is commonly connected. The connection point is connected to, e.g., a read word line RWLi (i = 1,..., j). The read word line RWLi runs in the Y-direction. One read word line RWLi is arranged in one column.

[0055] The MTJ elements 12 in the read blocks BKik arranged in one column are directly connected to the read word lines RWLi (i = 1,..., j) without intervening read select switches (MOS transistors). One end of each read word line RWLi is connected to a ground point VSS through a column select switch CSW formed from, e.g., a MOS transistor.

[0056] The column select switches CSW are arranged outside the memory cell array 11. Hence, no switch elements (MOS transistors) are arranged in the memory cell array 11.

[0057] The other terminal of each of the four MTJ elements 12 in the read block BKik is independently connected to a corresponding one of read bit lines RBL4(n-1)+1, RBL4(n-1)+2, RBL4(n-1)+3, and RBL4(n-1)+4. That is, the four read bit lines RBL4(n-1)+1, RBL4(n-1)+2, RBL4(n-1)+3, and RBL4(n-1)+4 are arranged in correspondence with the four MTJ elements 12 in one read block BKik.

[0058] The read bit lines RBL4(n-1)+1, RBL4(n-1)+2, RBL4(n-1)+3, and RBL4(n-1)+4 run in the X-direction. One end of each read bit line is connected to a common data line 30 through a row select switch (MOS transistor) RSW2. The common data line 30 is connected to a read circuit 29B (including, e.g., a sense amplifier, selector, and output buffer).

[0059] For example, as shown in FIGS. 111 and 121,

the read bit line is connected to a bias transistor BT which sets the bit line potential to VC.

[0060] A row select line signal RLi (i = 1,..., n) is input to each row select switch RSW2. Row decoders 25-1,..., 25-n output the row select line signals RLi.

[0061] As shown in FIG. 111, the bias transistor BT is a PMOS transistor, when the RLi is input to the bias transistor BT. As shown in FIG. 121, the bias transistor BT is a NMOS transistor, when the inverting signal from RLi is input to the bias transistor BT. Row decoders 25-1,..., 25-n output the row select line signals RLi and the inverting signal thereof.

[0062] The read bit lines RBL4(n-1)+1, RBL4(n-1)+2, RBL4(n-1)+3, and RBL4(n-1)+4 run in the X-direction and also function as write word lines WWL4(n-1)+1, WWL4(n-1)+2, WWL4(n-1)+3, and WWL4(n-1)+4, respectively.

[0063] One end of each of the write word lines WWL4 (n-1)+1, WWL4(n-1)+2, WWL4(n-1)+3, and WWL4(n-1) +4 is connected to a write word line driver 23A through the row select switches RSW2 and common data line 30. The other end of each write word line is connected to a corresponding one of write word line sinkers 24-1,.., 24-n.

[0064] One write bit line WBLi (i = 1,..., j) which is shared by the four MTJ elements 12 of one read block BKik and run in the Y-direction is arranged near the MTJ elements 12 constituting the read block BKik. One write bit line WBLi is arranged in one column.

[0065] One end of each write bit line WBLi is connected to a circuit block 29A including a column decoder and write bit line driver/sinker. The other end is connected to a circuit block 31 including a column decoder and write bit line driver/sinker.

[0066] In write operation, the circuit blocks 29A and 31 are set in an operative state. A write current flows to the write bit lines WBLi in accordance with write data in a direction toward the circuit block 29A or 31.

[0067] In the write operation, the row decoder 25-n selects one of the plurality of rows on the basis of a row address signal. The write word line driver 23A supplies a write current to the write word lines WWL4(n-1)+1, WWL4(n-1)+2, WWL4(n-1)+3, and WWL4(n-1)+4 in the selected row. The write current is absorbed by the write word line sinker 24-n.

[0068] In read operation, the row decoder 25-n selects one of the plurality of rows on the basis of a row address signal. In the read operation, a column decoder 32 selects one of the plurality of columns on the basis of column address signals CSL1,..., CSLj to turn on the column select switch CSW arranged in the selected column.

[0069] In the magnetic random access memory according to Structural Example 1, one terminal of each of the plurality of MTJ elements in a read block is commonly connected. The other terminal is connected to a corresponding one of different read bit lines RBL4(n-1)+1, RBL4(n-1)+2, RBL4(n-1)+3, and RBL4(n-1)+4.

[0070] Hence, data of the plurality of MTJ elements in one read block can be read at once by one read step.

[0071] The read bit lines RBL4(n-1)+1, RBL4(n-1)+2, RBL4(n-1)+3, and RBL4(n-1)+4 also function as the write word lines WWL4(n-1)+1, WWL4(n-1)+2, WWL4 (n-1)+3, and WWL4(n-1)+4, respectively. Since no interconnections which exclusively serve as write word lines need be arranged in the cell array, the cell array structure can be simplified.

[0072] As described above, as the characteristic feature of Structural Example 1, a read block has no read select switch for selecting it. In this case, the read bit lines RBL4(n-1)+1, RBL4(n-1)+2, RBL4(n-1)+3, and RBL4(n-1)+4 in an unselected row are biased to same potential to those in a selected row and the write word line WBLj in an unselected column is set in a floating state.

[0073] For this reason, the read bit lines RBL4(n-1) +1, RBL4(n-1)+2, RBL4(n-1)+3, and RBL4(n-1)+4 in all rows are set to the same potentials.

[0074] In Structural Example 1, in the read operation, for example, the potentials of the read bit lines RBL4(n-1)+1, RBL4(n-1)+2, RBL4(n-1)+3, and RBL4(n-1)+4 in the selected row are fixed to identical values. That is, the potentials of the read bit lines RBL4(n-1)+1, RBL4 (n-1)+2, RBL4(n-1)+3, and RBL4(n-1)+4 in the selected row are fixed, and a change in read current flowing to the MTJ elements is detected.

[0075] The circuit (clamp circuit) for fixing the potentials of the read bit lines RBL4(n-1)+1, RBL4(n-1)+2, RBL4(n-1)+3, and RBL4(n-1)+4 in the selected row will be described later in detail in association with a read circuit.

[0076] If the read bit lines RBL4(n-1)+1, RBL4(n-1) +2, RBL4(n-1)+3, and RBL4(n-1)+4 in all rows always have the same potential in the read operation, no sneak current flows between the read bit lines through the plurality of unselected MTJ elements and poses no problem in determining the data value of the selected MTJ element.

[0077] In Structural Example 1, since no read select transistor is arranged in the read block, a current path is formed through the MTJ elements in an unselected block in the read operation. However, the resistance value of the MTJ element is sufficiently large. The read current is much smaller than the write current. Hence, an increase in current consumption poses no serious problem.

[0078] In the write operation, when the write current flows to the write word lines WWL4(n-1)+1, WWL4(n-1) +2, WWL4(n-1)+3, and WWL4(n-1)+4 in the selected row, the read word line RWLi is charged through the MTJ elements in the selected row. The read word line RWLi is in the floating state. Hence, it is only charged. No potential difference is generated across the MTJ element.

② Device Structure 1

[0079] Device Structure 1 will be described next.

[1] Sectional Structure

[0080] FIG. 2 shows Device Structure 1 corresponding to one block of the magnetic random access memory according to Structural Example 1 of the present invention.

[0081] The same reference numerals as in FIG. 1 denote the same elements in FIG. 2 to show the correspondence between the elements.

[0082] A read word line RWL1 running in the Y-direction is formed on a semiconductor substrate 41. No switch element is arranged immediately under the read word line RWL1. Four MTJ elements (Magnetic Tunnel Junction elements) MTJ1, MTJ2, MTJ3, and MTJ4 arrayed in the Y-direction are formed above the read word line RWL1.

[0083] One terminal (upper end in this example) of each of the MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4 is commonly connected to an upper electrode 44. A contact plug 42 electrically connects the upper electrode 44 to the read word line RWL1.

[0084] The other terminal (lower end in this example) of each of the MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4 is electrically connected to a corresponding one of read bit lines RBL1, RBL2, RBL3, and RBL4 (write word lines WWL1, WWL2, WWL3, and WWL4). The read bit lines RBL1, RBL2, RBL3, and RBL4 run in the X-direction (row direction).

[0085] The MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4 are independently connected to the read bit lines RBL1, RBL2, RBL3, and RBL4, respectively. That is, the four read bit lines RBL1, RBL2, RBL3, and RBL4 are arranged in correspondence with the four MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4.

[0086] A write bit line WBL1 is formed above and near the MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4. The write bit line WBL1 runs in the Y-direction (column direction).

[0087] In Structural Example 1, one write bit line WBL1 is arranged in correspondence with the four MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4 which construct a read block. Instead, for example, the four MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4 may be stacked, and four write bit lines may be arranged in correspondence with the four MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4.

[0088] In Structural Example 1, the write bit line WBL1 running in the Y-direction is arranged above the MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4, and the read bit lines RBL1, RBL2, RBL3, and RBL4 running in the X-direction are arranged under the MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4.

[0089] However, the positional relationship of the write bit line WBL1 and read bit lines RBL1, RBL2, RBL3, and RBL4 with respect to the MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4 is not limited to this.

[0090] For example, the write bit line WBL1 running in the Y-direction may be arranged under the MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4, and the read bit lines RBL1, RBL2, RBL3, and RBL4 running in the X-direction are arranged above the MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4.

[0091] According to this device structure, the plurality of MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4 in the read block are electrically connected to the different read bit lines RBL1, RBL2, RBL3, and RBL4 (write word lines WWL1, WWL2, WWL3, and WWL4), respectively. For this reason, data of the plurality of MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4 in the read block can be read at once by one read step.

[0092] One terminal of each of the plurality of MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4 in the read block is commonly connected. The connection point is directly connected to the read word line RWL1 without intervening a read select switch. In addition, the write bit line WBL1 running in the Y-direction is shared by the plurality of MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4 in the read block. For this reason, the degree of integration of MTJ elements can be increased, and their characteristic can be improved.

[2] Plane Structure

[0093] FIG. 3 shows the positional relationship between the MTJ elements, the read bit lines (write word lines), and the write bit line in the device structure shown in FIG. 2.

[0094] The upper electrode 44 of the MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4 has, e.g., a rectangular shape and has, as a portion, a contact region for the contact plug.

[0095] The MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4 are arranged in the Y-direction. Their axis of easy magnetization (a direction parallel to the long sides of the MTJ elements) is the X-direction. That is, each of the MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4 has a rectangular shape long in the X-direction.

[0096] The MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4 are arranged in a region where the write bit line WBL1 and the read bit lines RBL1, RBL2, RBL3, and RBL4 (write word lines WWL1, WWL2, WWL3, and WWL4) cross each other.

③ Device Structure 2

[0097] Device Structure 2 will be described next.

[1] Sectional Structure

[0098] FIG. 4 shows Device Structure 2 corresponding to one block of the magnetic random access memory according to Structural Example 1 of the present inven-

tion.

[0099] The same reference numerals as in FIG. 1 denote the same elements in FIG. 4 to show the correspondence between the elements.

[0100] The read word line RWL1 running in the Y-direction is formed on the semiconductor substrate 41. No switch element is arranged immediately under the read word line RWL1. The four MTJ elements (Magnetic Tunnel Junction elements) MTJ1, MTJ2, MTJ3, and MTJ4 arrayed in the Y-direction are formed above the read word line RWL1.

[0101] One terminal (upper end in this example) of each of the MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4 is commonly connected to the upper electrode 44. The contact plug 42 and a conductive layer 43 electrically connect the upper electrode 44 to the read word line RWL1.

[0102] Device Structure 2 is different from Device Structure 1 in the position where the contact plug 42 is formed. More specifically, in Device Structure 1, the contact plug 42 is formed at an end portion in the Y-direction. In Device Structure 2, the contact plug 42 is arranged at the central portion of the upper electrode 44.

[0103] When the MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4 are uniformly arranged to be symmetrical with respect to the contact plug 42, signal margin in the read operation due to the interconnection resistance or the like can be maximized.

[0104] The conductive layer 43 may be integrated with the upper electrode 44. That is, the conductive layer 43 and upper electrode 44 may be formed simultaneously using the same material.

[0105] The other terminal (lower end in this example) of each of the MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4 is electrically connected to a corresponding one of the read bit lines RBL1, RBL2, RBL3, and RBL4 (write word lines WWL1, WWL2, WWL3, and WWL4). The read bit lines RBL1, RBL2, RBL3, and RBL4 run in the X-direction (row direction).

[0106] The MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4 are independently connected to the read bit lines RBL1, RBL2, RBL3, and RBL4, respectively. That is, the four read bit lines RBL1, RBL2, RBL3, and RBL4 are arranged in correspondence with the four MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4.

[0107] The write bit line WBL1 is formed above and near the MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4. The write bit line WBL1 runs in the Y-direction (column direction).

[0108] In Structural Example 1, one write bit line WBL1 is arranged in correspondence with the four MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4 which construct a read block. Instead, for example, the four MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4 may be stacked, and four write bit lines may be arranged in correspondence with the four MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4.

[0109] In Structural Example 1, the write bit line WBL1 running in the Y-direction is arranged above the MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4, and the read bit lines RBL1, RBL2, RBL3, and RBL4 running in the X-direction are arranged under the MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4.

[0110] However, the positional relationship of the write bit line WBL1 and read bit lines RBL1, RBL2, RBL3, and RBL4 with respect to the MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4 is not limited to this.

[0111] For example, the write bit line WBL1 running in the Y-direction may be arranged under the MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4, and the read bit lines RBL1, RBL2, RBL3, and RBL4 running in the X-direction are arranged above the MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4.

[0112] According to this device structure, the plurality of MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4 in the read block are electrically connected to the different read bit lines RBL1, RBL2, RBL3, and RBL4 (write word lines WWL1, WWL2, WWL3, and WWL4), respectively. For this reason, data of the plurality of MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4 in the read block can be read at once by one read step.

[0113] One terminal of each of the plurality of MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4 in the read block is commonly connected. The connection point is directly connected to the read word line RWL1 without intervening a read select switch. In addition, the write bit line WBL1 running in the Y-direction is shared by the plurality of MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4 in the read block. For this reason, the degree of integration of MTJ elements can be increased, and their characteristic can be improved.

[2] Plane Structure

[0114] FIGS. 5 to 7 show the layouts of the respective interconnection layers in Device Structure 2 shown in FIG. 4. The section shown in FIG. 4 corresponds to the section taken along a line IV - IV in FIGS. 5 to 7.

[0115] FIG. 5 shows the layout of read word lines.

[0116] The read word lines RWL1 run in the Y-direction. The contact plug 42 is arranged on each read word line RWL1.

[0117] FIG. 6 shows the layout of the read bit lines and MTJ elements.

[0118] The read bit lines RBL1, RBL2, RBL3, and RBL4 (write word lines WWL1, WWL2, WWL3, and WWL4) run in the X-direction. The interval between the read bit lines RBL1, RBL2, RBL3, and RBL4 can be set to, e.g., the minimum size (or design rule) processible by photolithography.

[0119] The MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4 are arranged on the read bit lines RBL1, RBL2, RBL3, and RBL4, respectively. The axis of easy magnetization of the MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4, i.e., the direction parallel to the long sides of the MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4 is the X-

direction.

[0120] The read bit line RBL1 is commonly connected to the MTJ elements MTJ1 arranged in the X-direction. The read bit line RBL2 is commonly connected to the MTJ elements MTJ2 arranged in the X-direction. The read bit line RBL3 is commonly connected to the MTJ elements MTJ3 arranged in the X-direction. The read bit line RBL4 is commonly connected to the MTJ elements MTJ4 arranged in the X-direction.

[0121] The conductive layer 43 is arranged on the contact plug 42.

[0122] FIG. 7 shows the layout of write bit lines.

[0123] The upper electrode 44 having a rectangular pattern is arranged on the MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4 and conductive layer 43. The upper electrode 44 are in contact with the MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4 and conductive layer 43.

[0124] The write bit lines WBL1 are arranged immediately on the upper electrodes 44. The write bit lines WBL1 run in the Y-direction.

④ Device Structure 3

[0125] Device Structure 3 will be described next.

[1] Sectional Structure

[0126] FIG. 8 shows Device Structure 3 corresponding to one block of the magnetic random access memory according to Structural Example 1 of the present invention.

[0127] The same reference numerals as in FIG. 1 denote the same elements in FIG. 8 to show the correspondence between the elements.

[0128] The write bit line WBL1 running in the Y-direction is formed on the semiconductor substrate 41. No switch element is arranged immediately under the write bit line WBL1. A lower electrode 44 having, e.g., a rectangular pattern is formed above the write bit line WBL1.

[0129] The four MTJ elements (Magnetic Tunnel Junction elements) MTJ1, MTJ2, MTJ3, and MTJ4 arrayed in the Y-direction are formed on the lower electrode 44.

[0130] The read bit lines RBL1, RBL2, RBL3, and RBL4 (write word lines WWL1, WWL2, WWL3, and WWL4) are formed on the MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4, respectively. The read bit lines RBL1, RBL2, RBL3, and RBL4 are in contact with the MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4, respectively. The read bit lines RBL1, RBL2, RBL3, and RBL4 run in the X-direction (row direction).

[0131] The MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4 are independently connected to the read bit lines RBL1, RBL2, RBL3, and RBL4, respectively. That is, the four read bit lines RBL1, RBL2, RBL3, and RBL4 are arranged in correspondence with the four MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4.

[0132] The contact plug 42 and conductive layer 43 are formed on the lower electrode 44. The contact plug 42 and conductive layer 43 electrically connect the lower electrode 44 to the read word line RWL1.

[0133] The contact plug 42 is arranged at the central portion of the lower electrode 44. When the MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4 are uniformly arranged to be symmetrical with respect to the contact plug 42, signal margin in the read operation due to the interconnection resistance or the like can be maximized.

[0134] The read word line RWL1 is formed above the MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4. The read word line RWL1 runs in the Y-direction (column direction).

[0135] In Structural Example 1, one write bit line WBL1 is arranged in correspondence with the four MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4 which construct a read block. Instead, for example, the four MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4 may be stacked, and four write bit lines may be arranged in correspondence with the four MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4.

[0136] In Structural Example 1, the write bit line WBL1 running in the Y-direction is arranged under the MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4, and the read bit lines RBL1, RBL2, RBL3, and RBL4 running in the X-direction are arranged above the MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4.

[0137] However, the positional relationship of the write bit line WBL1 and read bit lines RBL1, RBL2, RBL3, and RBL4 with respect to the MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4 is not limited to this.

[0138] For example, the write bit line WBL1 running in the Y-direction may be arranged above the MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4, and the read bit lines RBL1, RBL2, RBL3, and RBL4 running in the X-direction are arranged under the MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4.

[0139] According to this device structure, the plurality of MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4 in the read block are electrically connected to the different read bit lines RBL1, RBL2, RBL3, and RBL4 (write word lines WWL1, WWL2, WWL3, and WWL4), respectively. For this reason, data of the plurality of MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4 in the read block can be read at once by one read step.

[0140] One terminal of each of the plurality of MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4 in the read block is commonly connected. The connection point is directly connected to the read word line RWL1 without intervening a read select switch. In addition, the write bit line WBL1 running in the Y-direction is shared by the plurality of MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4 in the read block. For this reason, the degree of integration of MTJ elements can be increased, and their characteristic can be improved.

[0141] Furthermore, the contact portion between the lower electrode 44 and the read word line RWL1 is formed in the region between the MTJ elements MTJ1

and MTJ2 and the MTJ elements MTJ3 and MTJ4. When the MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4 are uniformly arranged to be symmetrical with respect to the contact portion of the lower electrode 44, signal margin in the read operation due to the interconnection resistance or the like can be maximized.

[2] Plane Structure

[0142] FIGS. 9 to 12 show the layouts of the respective interconnection layers in Device Structure 3 shown in FIG. 8. The section shown in FIG. 8 corresponds to the section taken along a line VIII - VIII in FIGS. 9 to 12.

[0143] FIG. 9 shows the layout of write bit lines.

[0144] The write bit lines WBL1 run in the Y-direction. The lower electrode 44 having a rectangular shape is arranged on each write bit line WBL1.

[0145] FIG. 10 shows the layout of MTJ elements.

[0146] The MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4 and conductive layer 43 are arranged on the lower electrode 44 having a rectangular pattern.

[0147] The MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4 on the lower electrode 44 are arranged in the Y-direction. The axis of easy magnetization of the MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4, i.e., the direction parallel to the long sides of the MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4 is the X-direction.

[0148] FIG. 11 shows the layout of read bit lines.

[0149] The read bit lines RBL1, RBL2, RBL3, and RBL4 (write word lines WWL1, WWL2, WWL3, and WWL4) are arranged on the MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4, respectively.

[0150] The read bit lines RBL1, RBL2, RBL3, and RBL4 run in the X-direction. The interval between the read bit lines RBL1, RBL2, RBL3, and RBL4 can be set to, e.g., the minimum size (or design rule) processible by photolithography.

[0151] The read bit line RBL1 is commonly connected to the MTJ elements MTJ1 arranged in the X-direction. The read bit line RBL2 is commonly connected to the MTJ elements MTJ2 arranged in the X-direction. The read bit line RBL3 is commonly connected to the MTJ elements MTJ3 arranged in the X-direction. The read bit line RBL4 is commonly connected to the MTJ elements MTJ4 arranged in the X-direction.

[0152] The contact plug 42 is arranged on the conductive layer 43.

[0153] FIG. 12 shows the layout of read word lines.

[0154] The read word lines RWL1 run in the Y-direction. The read word line RWL1 is in contact with the contact plug 42.

(2) Structural Example 2

① Outline

[0155] FIG. 13 shows the outline of a magnetic random access memory according to Structural Example 2 of the present invention.

[0156] The same reference numerals as in FIG. 1 denote the same elements in FIG. 13 to show the correspondence between the elements.

[0157] As a characteristic feature of Structural Example 2, a plurality of stages of memory cell arrays 11-1, 11-2,..., 11-m according to Structural Example 1 are stacked on a semiconductor substrate (chip) 10. Each of the memory cell arrays 11-1, 11-2,..., 11-m corresponds to the memory cell array 11 shown in FIG. 1.

② Device Structure 1

[0158] In Device Structure 1 of Structural Example 2, a plurality of stages of memory cell arrays in Device Structure 2 (FIG. 4) of Structural Example 1 are stacked.

[0159] FIG. 14 shows Device Structure 1 corresponding to one block of the magnetic random access memory according to Structural Example 2 of the present invention.

[1] First Stage (Memory Cell Array 11-1)

[0160] A read word line RWL1-1 running in the Y-direction is formed on a semiconductor substrate 41. No switch element is arranged immediately under the read word line RWL1-1. Four MTJ elements (Magnetic Tunnel Junction elements) MTJ1-1, MTJ2-1, MTJ3-1, and MTJ4-1 arrayed in the Y-direction are formed above the read word line RWL1-1.

[0161] One terminal (upper end in this example) of each of the MTJ elements MTJ1-1, MTJ2-1, MTJ3-1, and MTJ4-1 is commonly connected to an upper electrode 44-1. A contact plug 42-1 and conductive layer 43-1 electrically connect the upper electrode 44-1 to the read word line RWL1-1.

[0162] The contact plug 42-1 is arranged at the central portion of the upper electrode 44-1. When the MTJ elements MTJ1-1, MTJ2-1, MTJ3-1, and MTJ4-1 are uniformly arranged to be symmetrical with respect to the contact plug 42-1, signal margin in the read operation due to the interconnection resistance or the like can be maximized.

[0163] The conductive layer 43-1 may be integrated with the upper electrode 44-1. That is, the conductive layer 43-1 and upper electrode 44-1 may be formed simultaneously using the same material.

[0164] The other terminal (lower end in this example) of each of the MTJ elements MTJ1-1, MTJ2-1, MTJ3-1, and MTJ4-1 is electrically connected to a corresponding one of read bit lines RBL1-1, RBL2-1, RBL3-1, and RBL4-1 (write word lines WWL1-1, WWL2-1, WWL3-1, and WWL4-1). The read bit lines RBL1-1, RBL2-1, RBL3-1, and RBL4-1 run in the X-direction (row direction).

[0165] The MTJ elements MTJ1-1, MTJ2-1, MTJ3-1, and MTJ4-1 are independently connected to the read bit lines RBL1-1, RBL2-1, RBL3-1, and RBL4-1, respec-

tively. That is, the four read bit lines RBL1-1, RBL2-1, RBL3-1, and RBL4-1 are arranged in correspondence with the four MTJ elements MTJ1-1, MTJ2-1, MTJ3-1, and MTJ4-1.

[0166] A write bit line WBL1-1 is formed above and near the MTJ elements MTJ1-1, MTJ2-1, MTJ3-1, and MTJ4-1. The write bit line WBL1-1 runs in the Y-direction (column direction).

[2] Second Stage (Memory Cell Array 11-2)

[0167] A read word line RWL1-2 running in the Y-direction is formed on the write bit line WBL1-1 in the memory cell array 11-1 of the first stage. Four MTJ elements (Magnetic Tunnel Junction elements) MTJ1-2, MTJ2-2, MTJ3-2, and MTJ4-2 arrayed in the Y-direction are formed above the read word line RWL1-2.

[0168] One terminal (upper end in this example) of each of the MTJ elements MTJ1-2, MTJ2-2, MTJ3-2, and MTJ4-2 is commonly connected to an upper electrode 44-2. A contact plug 42-2 and conductive layer 43-2 electrically connect the upper electrode 44-2 to the read word line RWL1-2.

[0169] The contact plug 42-2 is arranged at the central portion of the upper electrode 44-2. When the MTJ elements MTJ1-2, MTJ2-2, MTJ3-2, and MTJ4-2 are uniformly arranged to be symmetrical with respect to the contact plug 42-2, signal margin in the read operation due to the interconnection resistance or the like can be maximized.

[0170] The conductive layer 43-2 may be integrated with the upper electrode 44-2. That is, the conductive layer 43-2 and upper electrode 44-2 may be formed simultaneously using the same material.

[0171] The other terminal (lower end in this example) of each of the MTJ elements MTJ1-2, MTJ2-2, MTJ3-2, and MTJ4-2 is electrically connected to a corresponding one of read bit lines RBL1-2, RBL2-2, RBL3-2, and RBL4-2 (write word lines WWL1-2, WWL2-2, WWL3-2, and WWL4-2). The read bit lines RBL1-2, RBL2-2, RBL3-2, and RBL4-2 run in the X-direction (row direction).

[0172] The MTJ elements MTJ1-2, MTJ2-2, MTJ3-2, and MTJ4-2 are independently connected to the read bit lines RBL1-2, RBL2-2, RBL3-2, and RBL4-2, respectively. That is, the four read bit lines RBL1-2, RBL2-2, RBL3-2, and RBL4-2 are arranged in correspondence with the four MTJ elements MTJ1-2, MTJ2-2, MTJ3-2, and MTJ4-2.

[0173] A write bit line WBL1-2 is formed above and near the MTJ elements MTJ1-2, MTJ2-2, MTJ3-2, and MTJ4-2. The write bit line WBL1-2 runs in the Y-direction (column direction).

[3] Others

[0174] Referring to FIG. 14, the memory cell arrays 11-1 and 11-2 according to Device Structure 2 of the Structural Example 1 are stacked in two stages on the semiconductor substrate 41. In principle, the memory cell arrays may be stacked in three or more stages (there is no upper limit).

[0175] According to Device Structure 1 of Structural Example 2, a plurality of stages of memory cell arrays according to Device Structure 2 of Structural Example 1 are stacked on the semiconductor substrate. For this reason, the density of MTJ elements can be increased.

③ Device Structure 2

[0176] In Device Structure 2 of Structural Example 2, a plurality of stages of memory cell arrays in Device Structure 3 (FIG. 8) of Structural Example 1 are stacked.

[0177] FIG. 15 shows Device Structure 2 corresponding to one block of the magnetic random access memory according to Structural Example 2 of the present invention.

[1] First Stage (Memory Cell Array 11-1)

[0178] The write bit line WBL1-1 running in the Y-direction is formed on the semiconductor substrate 41. No switch element is arranged immediately under the write bit line WBL1-1. A lower electrode 44-1 having, e.g., a rectangular pattern is formed above the write bit line WBL1-1.

[0179] The four MTJ elements (Magnetic Tunnel Junction elements) MTJ1-1, MTJ2-1, MTJ3-1, and MTJ4-1 arrayed in the Y-direction are formed on the lower electrode 44-1.

[0180] The read bit lines RBL1-1, RBL2-1, RBL3-1, and RBL4-1 (write word lines WWL1-1, WWL2-1, WWL3-1, and WWL4-1) are formed on the MTJ elements MTJ1-1, MTJ2-1, MTJ3-1, and MTJ4-1, respectively. The read bit lines RBL1-1, RBL2-1, RBL3-1, and RBL4-1 are in contact with the MTJ elements MTJ1-1, MTJ2-1, MTJ3-1, and MTJ4-1, respectively. The read bit lines RBL1-1, RBL2-1, RBL3-1, and RBL4-1 run in the X-direction (row direction).

[0181] The MTJ elements MTJ1-1, MTJ2-1, MTJ3-1, and MTJ4-1 are independently connected to the read bit lines RBL1-1, RBL2-1, RBL3-1, and RBL4-1, respectively. That is, the four read bit lines RBL1-1, RBL2-1, RBL3-1, and RBL4-1 are arranged in correspondence with the four MTJ elements MTJ1-1, MTJ2-1, MTJ3-1, and MTJ4-1.

[0182] The contact plug 42-1 and conductive layer 43-1 are formed on the lower electrode 44-1. The contact plug 42-1 and conductive layer 43-1 electrically connect the lower electrode 44-1 to the read word line RWL1-1.

[0183] The contact plug 42-1 is arranged at the central portion of the lower electrode 44-1. When the MTJ elements MTJ1-1, MTJ2-1, MTJ3-1, and MTJ4-1 are uniformly arranged to be symmetrical with respect to the contact plug 42-1, signal margin in the read operation

due to the interconnection resistance or the like can be maximized.

[0184] The read word line RWL1-1 is formed above the MTJ elements MTJ1-1, MTJ2-1, MTJ3-1, and MTJ4-1. The read word line RWL1-1 runs in the Y-direction (column direction).

[2] Second Stage (Memory Cell Array 11-2)

[0185] The write bit line WBL1-2 running in the Y-direction is formed on the semiconductor substrate 41. No switch element is arranged immediately under the write bit line WBL1-2. A lower electrode 44-2 having, e.g., a rectangular pattern is formed above the write bit line WBL1-2.

[0186] The four MTJ elements (Magnetic Tunnel Junction elements) MTJ1-2, MTJ2-2, MTJ3-2, and MTJ4-2 arrayed in the Y-direction are formed on the lower electrode 44-2.

[0187] The read bit lines RBL1-2, RBL2-2, RBL3-2, and RBL4-2 (write word lines WWL1-2, WWL2-2, WWL3-2, and WWL4-2) are formed on the MTJ elements MTJ1-2, MTJ2-2, MTJ3-2, and MTJ4-2, respectively. The read bit lines RBL1-2, RBL2-2, RBL3-2, and RBL4-2 are in contact with the MTJ elements MTJ1-2, MTJ2-2, MTJ3-2, and MTJ4-2, respectively. The read bit lines RBL1-2, RBL2-2, RBL3-2, and RBL4-2 run in the X-direction (row direction).

[0188] The MTJ elements MTJ1-2, MTJ2-2, MTJ3-2, and MTJ4-2 are independently connected to the read bit lines RBL1-2, RBL2-2, RBL3-2, and RBL4-2, respectively. That is, the four read bit lines RBL1-2, RBL2-2, RBL3-2, and RBL4-2 are arranged in correspondence with the four MTJ elements MTJ1-2, MTJ2-2, MTJ3-2, and MTJ4-2.

[0189] The contact plug 42-2 and conductive layer 43-2 are formed on the lower electrode 44-2. The contact plug 42-2 and conductive layer 43-2 electrically connect the lower electrode 44-2 to the read word line RWL1-2.

[0190] The contact plug 42-2 is arranged at the central portion of the lower electrode 44-2. When the MTJ elements MTJ1-2, MTJ2-2, MTJ3-2, and MTJ4-2 are uniformly arranged to be symmetrical with respect to the contact plug 42-2, signal margin in the read operation due to the interconnection resistance or the like can be maximized.

[0191] The read word line RWL1-2 is formed above the MTJ elements MTJ1-2, MTJ2-2, MTJ3-2, and MTJ4-2. The read word line RWL1-2 runs in the Y-direction (column direction).

[3] Others

[0192] Referring to FIG. 15, the memory cell arrays 11-1 and 11-2 according to Device Structure 3 of the Structural Example 1 are stacked in two stages on the semiconductor substrate 41. In principle, the memory cell arrays may be stacked in three or more stages (there is no upper limit).

[0193] According to Device Structure 2 of Structural Example 2, a plurality of stages of memory cell arrays according to Device Structure 3 of Structural Example 1 are stacked on the semiconductor substrate. For this reason, the density of MTJ elements can be increased.

(3) Structural Example 3

① Outline

[0194] Structural Example 3 is an improvement of Structural Example 2. In Structural Example 2, the plurality of stages of the memory cell arrays 11-1, 11-2,..., 11-m according to Structural Example 1 are stacked on the semiconductor substrate (chip).

[0195] Even in Structural Example 3, a plurality of stages of memory cell arrays according to Structural Example 1 are stacked on a semiconductor substrate (chip). In Structural Example 3, the number of interconnections in the memory cell arrays is decreased to planarize the underlying layer of MTJ elements (improve the characteristic of MTJ elements). For this purpose, one interconnection is shared by memory cell arrays of different stages.

② Circuit Structure

[0196] In Structural Example 3, in a plurality of stages of memory cell arrays 11-1, 11-2,..., 11-m stacked, as shown in FIG. 13, the write bit line of the memory cell array of the lower stage and the read word line of the memory cell array of the upper stage are integrated and shared as one write bit line/read word line.

[0197] FIGS. 16 and 17 show the main part of a magnetic random access memory according to Structural Example 3 of the present invention.

[1] First Stage (Lower Stage)

[0198] FIG. 16 shows the cell array structure of the first stage of Structural Example 3.

[0199] The memory cell array 11-1 has a plurality of MTJ elements 12 arranged in an array in the X- and Y-directions. For example, j MTJ elements 12 are arranged in the X-direction, and 4 × n MTJ elements 12 are arranged in the Y-direction.

[0200] The four MTJ elements 12 arranged in the Y-direction form one read block BKik (i = 1,..., j, and k = 1,..., n). One row is constructed by j read blocks BKik arranged in the X-direction. The memory cell array 11 has n rows. In addition, one column is constructed by n read blocks BKik arranged in the Y-direction. The memory cell array 11-1 has j columns.

[0201] One terminal of each of the four MTJ elements 12 in the block BKik is commonly connected. The connection point is connected to, e.g., a read word line RW-

Li-1 (i = 1,..., j). The read word line RWLi-1 runs in the Y-direction. One read word line RWLi-1 is arranged in one column.

[0202] The MTJ elements 12 in the read blocks BKik arranged in one column are directly connected to the read word lines RWLi-1 (i = 1,..., j) without intervening read select switches (MOS transistors). One end of each read word line RWLi-1 is connected to a ground point VSS through a column select switch CSW formed from, e.g., a MOS transistor.

[0203] The column select switches CSW are arranged outside the memory cell array 11-1. Hence, no switch elements (MOS transistors) are arranged in the memory cell array 11-1.

[0204] The other terminal of each of the four MTJ elements 12 in the read block BKik is independently connected to a corresponding one of read bit lines RBL{4(n-1)+1}-1, RBL{4(n-1)+2}-1, RBL{4(n-1)+3}-1, and RBL{4(n-1)+4}-1. That is, the four read bit lines RBL{4(n-1)+1}-1, RBL{4(n-1)+2}-1, RBL{4(n-1)+3}-1, and RBL{4(n-1)+4}-1 are arranged in correspondence with the four MTJ elements 12 in one read block BKik.

[0205] The read bit lines RBL{4(n-1)+1}-1, RBL{4(n-1)+2}-1, RBL{4(n-1)+3}-1, and RBL{4(n-1)+4}-1 run in the X-direction. One end of each read bit line is connected to a common data line 30(1) through a row select switch (MOS transistor) RSW2. The common data line 30(1) is connected to a read circuit 29B(1) (including, e.g., a sense amplifier, selector, and output buffer).

[0206] For example, as shown in FIGS. 112 and 122, the read bit line is connected to a bias transistor BT which sets the bit line potential to VC.

[0207] A row select line signal RLi (i = 1,..., n) is input to each row select switch RSW2. Row decoders 25(1)-1,..., 25(1)-n output the row select line signals RLi.

[0208] As shown in FIG. 112, the bias transistor BT is a PMOS transistor, when the RLi is input to the bias transistor BT. As shown in FIG. 122, the bias transistor BT is a NMOS transistor, when the inverting signal from RLi is input to the bias transistor BT. Row decoders 25(1)-1,..., 25(1)-n output the row select line signals RLi and the inverting signal thereof.

[0209] The read bit lines RBL{4(n-1)+1}-1, RBL{4(n-1)+2}-1, RBL{4(n-1)+3}-1, and RBL{4(n-1)+4}-1 run in the X-direction and also function as write word lines WWL{4(n-1)+1}-1, WWL{4(n-1)+2}-1, WWL{4(n-1)+3}-1, and WWL{4(n-1)+4}-1, respectively.

[0210] One end of each of the write word lines WWL{4(n-1)+1}-1, WWL{4(n-1)+2}-1, WWL{4(n-1)+3}-1, and WWL{4(n-1)+4}-1 is connected to a write word line driver 23A(1) through the row select switches RSW2 and common data line 30(1). The other end of each write word line is connected to a corresponding one of write word line sinkers 24(1)-1,.., 24(1)-n.

[0211] One write bit line WBLi-1 (i = 1,..., j) which is shared by the four MTJ elements 12 of one read block BKik and run in the Y-direction is arranged near the MTJ elements 12 constituting the read block BKik. One write bit line WBLi-1 is arranged in one column.

[0212] One end of each write bit line WBLi-1 is connected to a circuit block 29A(1) including a column decoder and write bit line driver/sinker through a switching circuit 22. The other end of the write bit line WBLi-1 is connected to a circuit block 31(1) including a column decoder and write bit line driver/sinker through a disconnecting circuit 21.

[0213] The disconnecting circuit 21 and switching circuit 22 are controlled by a memory cell array select signal SEL. In write operation, when the memory cell array 11-1 of the first stage (lower stage) is selected, the switching circuit 22 electrically connects one end of the write bit line WBLi-1 to the circuit block 29A(1). The disconnecting circuit 21 electrically connects the other end of the write bit line WBLi-1 to the circuit block 31(1).

[0214] In the write operation, the circuit blocks 29A(1) and 31(1) are set in an operative state. A write current flows to the write bit lines WBLi-1 in accordance with write data in a direction toward the circuit block 29A(1) or 31(1).

[0215] In the write operation, the row decoder 25(1)-n selects one of the plurality of rows on the basis of a row address signal. The write word line driver 23A(1) supplies a write current to the write word lines WWL{4(n-1)+1}-1, WWL{4(n-1)+2}-1, WWL{4(n-1)+3}-1, and WWL{4(n-1)+4}-1 in the selected row. The write current is absorbed by the write word line sinker 24(1)-n.

[0216] In read operation, the row decoder 25(1)-n selects one of the plurality of rows on the basis of a row address signal. In the read operation, a column decoder 32(1) selects one of the plurality of columns on the basis of column address signals CSL1,..., CSLj to turn on the column select switch CSW arranged in the selected column.

[2] Second Stage (Upper Stage)

[0217] FIG. 17 shows the cell array structure of the second stage of Structural Example 3.

[0218] The memory cell array 11-2 has the plurality of MTJ elements 12 arranged in an array in the X- and Y-directions. For example, j MTJ elements 12 are arranged in the X-direction, and 4 × n MTJ elements 12 are arranged in the Y-direction.

[0219] The four MTJ elements 12 arranged in the Y-direction form one read block BKik (i = 1,..., j, and k = 1,..., n). One row is constructed by j read blocks BKik arranged in the X-direction. The memory cell array 11 has n rows. In addition, one column is constructed by n read blocks BKik arranged in the Y-direction. The memory cell array 11-2 has j columns.

[0220] One terminal of each of the four MTJ elements 12 in the block BKik is commonly connected. The connection point is connected to, e.g., a read word line RWLi-2 (i = 1,..., j). The read word line RWLi-2 runs in the Y-direction. One read word line RWLi-2 is arranged in one column.

[0221] The MTJ elements 12 in the read blocks BKik arranged in one column are directly connected to the read word lines RWLi-2 (i = 1,..., j) without intervening read select switches (MOS transistors). One end of each read word line RWLi-2 is connected to the ground point VSS through the column select switch CSW formed from the switching circuit 22 and a MOS transistor.

[0222] The other end of the read word line RWLi-2 is connected to the circuit block 31(1) including a column decoder and write bit line driver/sinker through the disconnecting circuit 21.

[0223] The disconnecting circuit 21, switching circuit 22, and column select switches CSW are arranged outside the memory cell array 11-2. Hence, no switch elements (MOS transistors) are arranged in the memory cell array 11-2.

[0224] The disconnecting circuit 21 and switching circuit 22 are the disconnecting circuit 21 and switching circuit 22 in the cell array structure of the memory cell array of the first stage shown in FIG. 16.

[0225] The disconnecting circuit 21 and switching circuit 22 are controlled by the memory cell array select signal SEL.

[0226] As described above, in the write operation, when the memory cell array 11-1 of the first stage (lower stage) is selected, the switching circuit 22 electrically connects one end of the write bit line WBLi-1 to the circuit block 29A(1). The disconnecting circuit 21 electrically connects the other end of the write bit line WBLi-1 to the circuit block 31(1).

[0227] In the read operation, when the memory cell array 11-2 of the second stage (upper stage) is selected, the switching circuit 22 electrically connects one end of the read word line RWLi-2 to the column select switch CSW. The disconnecting circuit 21 electrically disconnects the other end of the read word line RWLi-2 from the circuit block 31(1).

[0228] The other terminal of each of the four MTJ elements 12 in the read block BKik is independently connected to a corresponding one of read bit lines RBL{4(n-1)+1}-2, RBL{4(n-1)+2}-2, RBL{4(n-1)+3}-2, and RBL{4(n-1)+4}-2. That is, the four read bit lines RBL{4(n-1)+1}-2, RBL{4(n-1)+2}-2, RBL{4(n-1)+3}-2, and RBL{4(n-1)+4}-2 are arranged in correspondence with the four MTJ elements 12 in one read block BKik.

[0229] The read bit lines RBL{4(n-1)+1}-2, RBL{4(n-1)+2}-2, RBL{4(n-1)+3}-2, and RBL{4(n-1)+4}-2 run in the X-direction. One end of each read bit line is connected to a common data line 30(2) through a row select switch (MOS transistor) RSW2. The common data line 30(2) is connected to a read circuit 29B(2) (including, e.g., a sense amplifier, selector, and output buffer).

[0230] For example, as shown in FIGS. 113 and 123, the read bit line is connected to a bias transistor BT which sets the bit line potential to VC.

[0231] A row select line signal RLi (i = 1,..., n) is input to each row select switch RSW2. Row decoders 25(2)-1,..., 25(2)-n output the row select line signals RLi.

[0232] As shown in FIG. 113, the bias transistor BT is a PMOS transistor, when the RLi is input to the bias transistor BT. As shown in FIG. 123, the bias transistor BT is a NMOS transistor, when the inverting signal from RLi is input to the bias transistor BT. Row decoders 25(2)-1,..., 25(2)-n output the row select line signals RLi and the inverting signal thereof.

[0233] The read bit lines RBL{4(n-1)+1}-2, RBL{4(n-1)+2}-2, RBL{4(n-1)+3}-2, and RBL{4(n-1)+4}-2 run in the X-direction and also function as write word lines WWL{4(n-1)+1}-2, WWL{4(n-1)+2}-2, WWL{4(n-1)+3}-2, and WWL{4(n-1)+4}-2, respectively.

[0234] One end of each of the write word lines WWL{4(n-1)+1}-2, WWL{4(n-1)+2}-2, WWL{4(n-1)+3}-2, and WWL{4(n-1)+4}-2 is connected to a write word line driver 23A(2) through the row select switches RSW2 and common data line 30(2). The other end of each write word line is connected to a corresponding one of write word line sinkers 24(2)-1,.., 24(2)-n.

[0235] One write bit line WBLi-2 (i = 1,..., j) which is shared by the four MTJ elements 12 of one read block BKik and run in the Y-direction is arranged near the MTJ elements 12 constituting the read block BKik. One write bit line WBLi-2 is arranged in one column.

[0236] One end of each write bit line WBLi-2 is connected to a circuit block 29A(2) including a column decoder and write bit line driver/sinker. The other end of the write bit line WBLi-2 is connected to a circuit block 31(2) including a column decoder and write bit line driver/sinker.

[0237] In the write operation, the circuit blocks 29A(2) and 31(2) are set in an operative state. A write current flows to the write bit lines WBLi-2 in accordance with write data in a direction toward the circuit block 29A(2) or 31(2).

[0238] In the write operation, the row decoder 25(2)-n selects one of the plurality of rows on the basis of a row address signal. The write word line driver 23A(2) supplies a write current to the write word lines WWL{4(n-1)+1}-2, WWL{4(n-1)+2}-2, WWL{4(n-1)+3}-2, and WWL{4(n-1)+4}-2 in the selected row. The write current is absorbed by the write word line sinker 24(2)-n.

[0239] In the read operation, the row decoder 25(2)-n selects one of the plurality of rows on the basis of a row address signal. In the read operation, a column decoder 32(2) selects one of the plurality of columns on the basis of column address signals CSL1,..., CSLj to turn on the column select switch CSW arranged in the selected column.

③ Device Structure (Sectional Structure)

[0240] As a characteristic feature of the device structure of Structural Example 3, in the memory cell array of Device Structure 1 (FIG. 14) of Structural Example 2, a write bit line WBL1-1 of the lower stage (first stage) and a read word line RWL1-2 of the upper stage (second

stage) are integrated and shared as one write bit line/read word line WBL1-1/RWL1-2.

[0241] FIG. 18 shows a device structure corresponding to one block of the magnetic random access memory according to Structural Example 3 of the present invention.

[1] First Stage (Memory Cell Array 11-1)

[0242] The read word line RWL1-1 running in the Y-direction is formed on a semiconductor substrate 41. No switch element is arranged immediately under the read word line RWL1-1. Four MTJ elements (Magnetic Tunnel Junction elements) MTJ1-1, MTJ2-1, MTJ3-1, and MTJ4-1 arrayed in the Y-direction are formed above the read word line RWL1-1.

[0243] One terminal (upper end in this example) of each of the MTJ elements MTJ1-1, MTJ2-1, MTJ3-1, and MTJ4-1 is commonly connected to an upper electrode 44-1. A contact plug 42-1 and conductive layer 43-1 electrically connect the upper electrode 44-1 to the read word line RWL1-1.

[0244] The contact plug 42-1 is arranged at the central portion of the upper electrode 44-1. When the MTJ elements MTJ1-1, MTJ2-1, MTJ3-1, and MTJ4-1 are uniformly arranged to be symmetrical with respect to the contact plug 42-1, signal margin in the read operation due to the interconnection resistance or the like can be maximized.

[0245] The conductive layer 43-1 may be integrated with the upper electrode 44-1. That is, the conductive layer 43-1 and upper electrode 44-1 may be formed simultaneously using the same material.

[0246] The other terminal (lower end in this example) of each of the MTJ elements MTJ1-1, MTJ2-1, MTJ3-1, and MTJ4-1 is electrically connected to a corresponding one of read bit lines RBL1-1, RBL2-1, RBL3-1, and RBL4-1 (write word lines WWL1-1, WWL2-1, WWL3-1, and WWL4-1). The read bit lines RBL1-1, RBL2-1, RBL3-1, and RBL4-1 run in the X-direction (row direction).

[0247] The MTJ elements MTJ1-1, MTJ2-1, MTJ3-1, and MTJ4-1 are independently connected to the read bit lines RBL1-1, RBL2-1, RBL3-1, and RBL4-1, respectively. That is, the four read bit lines RBL1-1, RBL2-1, RBL3-1, and RBL4-1 are arranged in correspondence with the four MTJ elements MTJ1-1, MTJ2-1, MTJ3-1, and MTJ4-1.

[0248] A write bit line WBL1-1 is formed above and near the MTJ elements MTJ1-1, MTJ2-1, MTJ3-1, and MTJ4-1. The write bit line WBL1-1 runs in the Y-direction (column direction).

[2] Second Stage (Memory Cell Array 11-2)

[0249] The write bit line WBL1-1 in the memory cell array 11-1 of the first stage also functions as the read word line RWL1-2 in the memory cell array 11-2 of the second stage.

[0250] More specifically, in the write operation, when the memory cell array 11-1 of the first stage is selected, the write bit line/read word line WBL1-1/RWL1-2 are used as the write bit line WBL1-1. In the read operation, when the memory cell array 11-2 of the second stage is selected, the write bit line/read word line WBL1-1/RWL1-2 is used as the read word line RWL1-2.

[0251] Four MTJ elements (Magnetic Tunnel Junction elements) MTJ1-2, MTJ2-2, MTJ3-2, and MTJ4-2 arrayed in the Y-direction are formed above the read word line RWL1-2.

[0252] One terminal (upper end in this example) of each of the MTJ elements MTJ1-2, MTJ2-2, MTJ3-2, and MTJ4-2 is commonly connected to an upper electrode 44-2. A contact plug 42-2 and conductive layer 43-2 electrically connect the upper electrode 44-2 to the read word line RWL1-2.

[0253] The contact plug 42-2 is arranged at the central portion of the upper electrode 44-2. When the MTJ elements MTJ1-2, MTJ2-2, MTJ3-2, and MTJ4-2 are uniformly arranged to be symmetrical with respect to the contact plug 42-2, signal margin in the read operation due to the interconnection resistance or the like can be maximized.

[0254] The conductive layer 43-2 may be integrated with the upper electrode 44-2. That is, the conductive layer 43-2 and upper electrode 44-2 may be formed simultaneously using the same material.

[0255] The other terminal (lower end in this example) of each of the MTJ elements MTJ1-2, MTJ2-2, MTJ3-2, and MTJ4-2 is electrically connected to a corresponding one of read bit lines RBL1-2, RBL2-2, RBL3-2, and RBL4-2 (write word lines WWL1-2, WWL2-2, WWL3-2, and WWL4-2). The read bit lines RBL1-2, RBL2-2, RBL3-2, and RBL4-2 run in the X-direction (row direction).

[0256] The MTJ elements MTJ1-2, MTJ2-2, MTJ3-2, and MTJ4-2 are independently connected to the read bit lines RBL1-2, RBL2-2, RBL3-2, and RBL4-2, respectively. That is, the four read bit lines RBL1-2, RBL2-2, RBL3-2, and RBL4-2 are arranged in correspondence with the four MTJ elements MTJ1-2, MTJ2-2, MTJ3-2, and MTJ4-2.

[0257] A write bit line WBL1-2 is formed above and near the MTJ elements MTJ1-2, MTJ2-2, MTJ3-2, and MTJ4-2. The write bit line WBL1-2 runs in the Y-direction (column direction).

[3] Others

[0258] In the example shown in FIG. 18, the memory cell arrays 11-1 and 11-2 are stacked in two stages on the semiconductor substrate 41. In principle, the memory cell arrays may be stacked in three or more stages (there is no upper limit).

[0259] According to the device structure of Structural Example 3, the memory cell array 11-1 of the lower

stage and the memory cell array 11-2 of the upper stage according to Device Structure 1 of Structural Example 2 share one interconnection. For this reason, the density of MTJ elements can be increased. In addition, the underlying layer of the MTJ elements can be planarized (the characteristic of the MTJ elements can be improved).

④ Device Structure (Plane Structure)

[0260] FIGS. 19 to 23 show the layouts of the respective interconnection layers in Device Structure 1 shown in FIG. 18. The section shown in FIG. 18 corresponds to the section taken along a line XVIII - XVIII in FIGS. 19 to 23.

[0261] FIG. 19 shows the layout of read word lines of the first stage.

[0262] The read word lines RWL1-1 run in the Y-direction. The contact plug 42-1 is arranged on each read word line RWL1-1.

[0263] FIG. 20 shows the layout of read bit lines of the first stage and MTJ elements of the first stage.

[0264] The read bit lines RBL1-1, RBL2-1, RBL3-1, and RBL4-1 (write word lines WWL1-1, WWL2-1, WWL3-1, and WWL4-1) run in the X-direction. The interval between the read bit lines RBL1-1, RBL2-1, RBL3-1, and RBL4-1 can be set to, e.g., the minimum size (or design rule) processible by photolithography.

[0265] The MTJ elements MTJ1-1, MTJ2-1, MTJ3-1, and MTJ4-1 are arranged on the read bit lines RBL1-1, RBL2-1, RBL3-1, and RBL4-1. The axis of easy magnetization of the MTJ elements MTJ1-1, MTJ2-1, MTJ3-1, and MTJ4-1, i.e., the direction parallel to the long sides of the MTJ elements MTJ1-1, MTJ2-1, MTJ3-1, and MTJ4-1 is the X-direction.

[0266] The read bit line RBL1-1 is commonly connected to the MTJ elements MTJ1-1 arranged in the X-direction. The read bit line RBL2-1 is commonly connected to the MTJ elements MTJ2-1 arranged in the X-direction. The read bit line RBL3-1 is commonly connected to the MTJ elements MTJ3-1 arranged in the X-direction. The read bit line RBL4-1 is commonly connected to the MTJ elements MTJ4-1 arranged in the X-direction.

[0267] The conductive layer 43-1 is arranged on the contact plug 42-1.

[0268] FIG. 21 shows the layout of write bit lines of the first stage/read word lines of the second stage.

[0269] The upper electrodes 44-1 each having a rectangular pattern are arranged on the MTJ elements MTJ1-1, MTJ2-1, MTJ3-1, and MTJ4-1 and conductive layers 43. The upper electrodes 44-1 are in contact with the MTJ elements MTJ1-1, MTJ2-1, MTJ3-1, and MTJ4-1 and conductive layers 43-1.

[0270] The write bit lines/read word lines WBL1-1/RWL1-2 are arranged immediately on the upper electrodes 44-1. The write bit lines/read word lines WBL1-1/RWL1-2 run in the Y-direction.

[0271] The contact plug 42-2 is arranged on each write bit lines/read word lines WBL1-1/RWL1-2.

[0272] FIG. 22 shows the layout of read bit lines of the second stage and MTJ elements of the second stage.

[0273] The read bit lines RBL1-2, RBL2-2, RBL3-2, and RBL4-2 (write word lines WWL1-2, WWL2-2, WWL3-2, and WWL4-2) run in the X-direction. The interval between the read bit lines RBL1-2, RBL2-2, RBL3-2, and RBL4-2 can be set to, e.g., the minimum size (or design rule) processible by photolithography.

[0274] The MTJ elements MTJ1-2, MTJ2-2, MTJ3-2, and MTJ4-2 are arranged on the read bit lines RBL1-2, RBL2-2, RBL3-2, and RBL4-2. The axis of easy magnetization of the MTJ elements MTJ1-2, MTJ2-2, MTJ3-2, and MTJ4-2, i.e., the direction parallel to the long sides of the MTJ elements MTJ1-2, MTJ2-2, MTJ3-2, and MTJ4-2 is the X-direction.

[0275] The read bit line RBL1-2 is commonly connected to the MTJ elements MTJ1-2 arranged in the X-direction. The read bit line RBL2-2 is commonly connected to the MTJ elements MTJ2-2 arranged in the X-direction. The read bit line RBL3-2 is commonly connected to the MTJ elements MTJ3-2 arranged in the X-direction. The read bit line RBL4-2 is commonly connected to the MTJ elements MTJ4-2 arranged in the X-direction.

[0276] The conductive layer 43-2 is arranged on the contact plug 42-2.

[0277] FIG. 23 shows the layout of write bit lines of the second stage.

[0278] The upper electrodes 44-2 each having a rectangular pattern are arranged on the MTJ elements MTJ1-2, MTJ2-2, MTJ3-2, and MTJ4-2 and conductive layer 43-2. The upper electrodes 44-2 are in contact with the MTJ elements MTJ1-2, MTJ2-2, MTJ3-2, and MTJ4-2 and conductive layers 43-2.

[0279] The write bit lines WBL1-2 are arranged immediately on the upper electrodes 44-2. The write bit lines WBL1-2 run in the Y-direction.

(4) Structural Example 4

① Outline

[0280] Structural Example 4 is also an improvement of Structural Example 2. In Structural Example 4, a plurality of stages of memory cell arrays are stacked on a semiconductor substrate (chip), and one interconnection is shared by memory cell arrays of different stages, as in Structural Example 3. With this arrangement, the number of interconnections in the memory cell arrays is decreased to planarize the underlying layer of MTJ elements (improve the characteristic of MTJ elements).

[0281] Structural Example 4 is different from Structural Example 3 in the positional relationship of an interconnection to be shared. More specifically, in Structural Example 3, one interconnection is shared as a write bit line of the memory cell array of the lower stage and a

read word line of the memory cell array of the upper stage. In Structural Example 4, one interconnection is shared as a read word line of the memory cell array of the lower stage and a write bit line of the memory cell array of the upper stage.

② Circuit Structure

[0282] In Structural Example 4, in a plurality of stages of memory cell arrays 11-1, 11-2,..., 11-m stacked, the read word line of the memory cell array of the lower stage and the write bit line of the memory cell array of the upper stage are integrated and shared as one write bit line/read word line.

[0283] FIGS. 24 and 25 show the main part of a magnetic random access memory according to Structural Example 4 of the present invention.

[1] First Stage (Lower Stage)

[0284] FIG. 24 shows the cell array structure of the first stage of Structural Example 4.

[0285] The memory cell array 11-1 has a plurality of MTJ elements 12 arranged in an array in the X- and Y-directions. For example, j MTJ elements 12 are arranged in the X-direction, and 4 × n MTJ elements 12 are arranged in the Y-direction.

[0286] The four MTJ elements 12 arranged in the Y-direction form one read block BKik (i = 1,..., j, and k = 1,..., n). One row is constructed by j read blocks BKik arranged in the X-direction. The memory cell array 11 has n rows. In addition, one column is constructed by n read blocks BKik arranged in the Y-direction. The memory cell array 11-1 has j columns.

[0287] One terminal of each of the four MTJ elements 12 in the block BKik is commonly connected. The connection point is connected to, e.g., a read word line RWLi-1 (i = 1,..., j). The read word line RWLi-1 runs in the Y-direction. One read word line RWLi-1 is arranged in one column.

[0288] The MTJ elements 12 in the read blocks BKik arranged in one column are directly connected to the read word lines RWLi-1 (i = 1,..., j) without intervening read select switches (MOS transistors). One end of each read word line RWLi-1 is connected to a ground point VSS through a switching circuit 22 and a column select switch CSW formed from a MOS transistor.

[0289] The other end of the read word line RWLi-1 is connected to a circuit block 31(2) including a column decoder and write bit line driver/sinker through a disconnecting circuit 21.

[0290] The disconnecting circuit 21, switching circuit 22, and column select switches CSW are arranged outside the memory cell array 11-1. Hence, no switch elements (MOS transistors) are arranged in the memory cell array 11-1.

[0291] The disconnecting circuit 21 and switching circuit 22 are controlled by a memory cell array select signal SEL.

[0292] For example, in read operation, when the memory cell array 11-1 of the first stage (lower stage) is selected, the switching circuit 22 electrically connects one end of the read word line RWLi-1 to the column select switch CSW. The disconnecting circuit 21 electrically disconnects the other end of the read word line RWLi-1 from the circuit block 31(2).

[0293] The other terminal of each of the four MTJ elements 12 in the read block BKik is independently connected to a corresponding one of read bit lines RBL{4(n-1)+1}-1, RBL{4(n-1)+2}-1, RBL{4(n-1)+3}-1, and RBL{4(n-1)+4}-1. That is, the four read bit lines RBL{4(n-1)+1}-1, RBL{4(n-1)+2}-1, RBL{4(n-1)+3}-1, and RBL{4(n-1)+4}-1 are arranged in correspondence with the four MTJ elements 12 in one read block BKik.

[0294] The read bit lines RBL{4(n-1)+1}-1, RBL{4(n-1)+2}-1, RBL{4(n-1)+3}-1, and RBL{4(n-1)+4}-1 run in the X-direction. One end of each read bit line is connected to a common data line 30(1) through a row select switch (MOS transistor) RSW2. The common data line 30(1) is connected to a read circuit 29B(1) (including, e.g., a sense amplifier, selector, and output buffer).

[0295] For example, as shown in FIGS. 114 and 124, the read bit line is connected to a bias transistor BT which sets the bit line potential to VC.

[0296] A row select line signal RLi (i = 1,..., n) is input to each row select switch RSW2. Row decoders 25(1)-1,..., 25(1)-n output the row select line signals RLi.

[0297] As shown in FIG. 114, the bias transistor BT is a PMOS transistor, when the RLi is input to the bias transistor BT. As shown in FIG. 124, the bias transistor BT is a NMOS transistor, when the inverting signal from RLi is input to the bias transistor BT. Row decoders 25(1)-1,..., 25(1)-n output the row select line signals RLi and the inverting signal thereof.

[0298] The read bit lines RBL{4(n-1)+1}-1, RBL{4(n-1)+2}-1, RBL{4(n-1)+3}-1, and RBL{4(n-1)+4}-1 run in the X-direction and also function as write word lines WWL{4(n-1)+1}-1, WWL{4(n-1)+2}-1, WWL{4(n-1)+3}-1, and WWL{4(n-1)+4}-1, respectively.

[0299] One end of each of the write word lines WWL{4(n-1)+1}-1, WWL{4(n-1)+2}-1, WWL{4(n-1)+3}-1, and WWL{4(n-1)+4}-1 is connected to a write word line driver 23A(1) through the row select switches RSW2 and common data line 30(1). The other end of each write word line is connected to a corresponding one of write word line sinkers 24(1)-1,.., 24(1)-n.

[0300] One write bit line WBLi-1 (i = 1,..., j) which is shared by the four MTJ elements 12 of one read block BKik and run in the Y-direction is arranged near the MTJ elements 12 constituting the read block BKik. One write bit line WBLi-1 is arranged in one column.

[0301] One end of each write bit line WBLi-1 is connected to a circuit block 29A(1) including a column decoder and write bit line driver/sinker. The other end of the write bit line WBLi-1 is connected to a circuit block 31(1) including a column decoder and write bit line driv-

er/sinker.

[0302] In the write operation, the circuit blocks 29A(1) and 31(1) are set in an operative state. A write current flows to the write bit lines WBLi-2 in accordance with write data in a direction toward the circuit block 29A(1) or 31(1).

[0303] In the write operation, the row decoder 25(1)-n selects one of the plurality of rows on the basis of a row address signal. The write word line driver 23A(1) supplies a write current to the write word lines WWL{4(n-1)+1}-1, WWL{4(n-1)+2}-1, WWL{4(n-1)+3}-1, and WWL{4(n-1)+4}-1 in the selected row. The write current is absorbed by the write word line sinker 24(1)-n.

[0304] In read operation, the row decoder 25(1)-n selects one of the plurality of rows on the basis of a row address signal. In the read operation, a column decoder 32(1) selects one of the plurality of columns on the basis of column address signals CSL1,..., CSLj to turn on the column select switch CSW arranged in the selected column.

[2] Second Stage (Upper Stage)

[0305] FIG. 25 shows the cell array structure of the second stage of Structural Example 4.

[0306] The memory cell array 11-2 has the plurality of MTJ elements 12 arranged in an array in the X- and Y-directions. For example, j MTJ elements 12 are arranged in the X-direction, and 4 × n MTJ elements 12 are arranged in the Y-direction.

[0307] The four MTJ elements 12 arranged in the Y-direction form one read block BKik (i = 1,..., j, and k = 1,..., n). One row is constructed by j read blocks BKik arranged in the X-direction. The memory cell array 11 has n rows. In addition, one column is constructed by n read blocks BKik arranged in the Y-direction. The memory cell array 11-2 has j columns.

[0308] One terminal of each of the four MTJ elements 12 in the block BKik is commonly connected. The connection point is connected to, e.g., a read word line RWLi-2 (i = 1,..., j). The read word line RWLi-2 runs in the Y-direction. One read word line RWLi-2 is arranged in one column.

[0309] The MTJ elements 12 in the read blocks BKik arranged in one column are directly connected to the read word lines RWLi-2 (i = 1,..., j) without intervening read select switches (MOS transistors). One end of each read word line RWLi-2 is connected to the ground point VSS through the column select switch CSW formed from, e.g., a MOS transistor.

[0310] The column select switches CSW are arranged outside the memory cell array 11-2. Hence, no switch elements (MOS transistors) are arranged in the memory cell array 11-2.

[0311] The other terminal of each of the four MTJ elements 12 in the read block BKik is independently connected to a corresponding one of read bit lines RBL{4(n-1)+1}-2, RBL{4(n-1)+2}-2, RBL{4(n-1)+3}-2, and RBL{4(n-1)+4}-2. That is, the four read bit lines RBL{4(n-1)+1}-2, RBL{4(n-1)+2}-2, RBL{4(n-1)+3}-2, and RBL{4(n-1)+4}-2 are arranged in correspondence with the four MTJ elements 12 in one read block BKik.

[0312] The read bit lines RBL{4(n-1)+1}-2, RBL{4(n-1)+2}-2, RBL{4(n-1)+3}-2, and RBL{4(n-1)+4}-2 run in the X-direction. One end of each read bit line is connected to a common data line 30(2) through a row select switch (MOS transistor) RSW2. The common data line 30(2) is connected to a read circuit 29B(2) (including, e.g., a sense amplifier, selector, and output buffer).

[0313] For example, as shown in FIGS. 115 and 125, the read bit line is connected to a bias transistor BT which sets the bit line potential to VC.

[0314] A row select line signal RLi (i = 1,..., n) is input to each row select switch RSW2. Row decoders 25(2)-1,..., 25(2)-n output the row select line signals RLi.

[0315] As shown in FIG. 115, the bias transistor BT is a PMOS transistor, when the RLi is input to the bias transistor BT. As shown in FIG. 125, the bias transistor BT is a NMOS transistor, when the inverting signal from RLi is input to the bias transistor BT. Row decoders 25(2)-1,..., 25(2)-n output the row select line signals RLi and the inverting signal thereof.

[0316] The read bit lines RBL{4(n-1)+1}-2, RBL{4(n-1)+2}-2, RBL{4(n-1)+3}-2, and RBL{4(n-1)+4}-2 run in the X-direction and also function as write word lines WWL{4(n-1)+1}-2, WWL{4(n-1)+2}-2, WWL{4(n-1)+3}-2, and WWL{4(n-1)+4}-2, respectively.

[0317] One end of each of the write word lines WWL{4(n-1)+1}-2, WWL{4(n-1)+2}-2, WWL{4(n-1)+3}-2, and WWL{4(n-1)+4}-2 is connected to a write word line driver 23A(2) through the row select switches RSW2 and common data line 30(2). The other end of each write word line is connected to a corresponding one of write word line sinkers 24(2)-1,.., 24(2)-n.

[0318] One write bit line WBLi-2 (i = 1,..., j) which is shared by the four MTJ elements 12 of one read block BKik and run in the Y-direction is arranged near the MTJ elements 12 constituting the read block BKik. One write bit line WBLi-2 is arranged in one column.

[0319] One end of each write bit line WBLi-2 is connected to a circuit block 29A(2) including a column decoder and write bit line driver/sinker through the switching circuit 22. The other end of the write bit line WBLi-2 is connected to a circuit block 31(2) including a column decoder and write bit line driver/sinker through the disconnecting circuit 21.

[0320] The disconnecting circuit 21 and switching circuit 22 are the disconnecting circuit 21 and switching circuit 22 in the cell array structure of the memory cell array of the first stage shown in FIG. 24.

[0321] The disconnecting circuit 21 and switching circuit 22 are controlled by the memory cell array select signal SEL.

[0322] As described above, in the read operation, when the memory cell array 11-1 of the first stage (lower stage) is selected, the switching circuit 22 electrically

connects one end of the read word line RWLi-1 to the column select switch CSW. The disconnecting circuit 21 electrically disconnects the other end of the read word line RWLi-1 from the circuit block 31(2).

[0323] In the write operation, when the memory cell array 11-2 of the second stage (upper stage) is selected, the switching circuit 22 electrically connects one end of the write bit line WBLi-2 to the circuit block 29A(2). The disconnecting circuit 21 electrically connects the other end of the write bit line WBLi-2 to the circuit block 31(2).

[0324] In the write operation, the circuit blocks 29A(2) and 31(2) are set in an operative state. A write current flows to the write bit lines WBLi-2 in accordance with write data in a direction toward the circuit block 29A(2) or 31(2).

[0325] In the write operation, the row decoder 25(2)-n selects one of the plurality of rows on the basis of a row address signal. The write word line driver 23A(2) supplies a write current to the write word lines WWL{4(n-1)+1}-2, WWL{4(n-1)+2}-2, WWL{4(n-1)+3}-2, and WWL{4(n-1)+4}-2 in the selected row. The write current is absorbed by the write word line sinker 24(2)-n.

[0326] In the read operation, the row decoder 25(2)-n selects one of the plurality of rows on the basis of a row address signal. In the read operation, a column decoder 32(2) selects one of the plurality of columns on the basis of column address signals CSL1,..., CSLj to turn on the column select switch CSW arranged in the selected column.

③ Device Structure (Sectional Structure)

[0327] As a characteristic feature of the device structure of Structural Example 4, in the memory cell array of Device Structure 2 (FIG. 15) of Structural Example 2, a read word line RWL1-1 of the lower stage (first stage) and a write bit line WBL1-2 of the upper stage (second stage) are integrated and shared as one read word line/write bit line RWL1-1/WBL1-2.

[0328] FIG. 26 shows a device structure corresponding to one block of the magnetic random access memory according to Structural Example 4 of the present invention.

[1] First Stage (Memory Cell Array 11-1)

[0329] The write bit line WBL1-1 running in the Y-direction is formed on a semiconductor substrate 41. No switch element is arranged immediately under the write bit line WBL1-1. A lower electrode 44-1 having, e.g., a rectangular pattern is formed above the write bit line WBL1-1.

[0330] The four MTJ elements (Magnetic Tunnel Junction elements) MTJ1-1, MTJ2-1, MTJ3-1, and MTJ4-1 arrayed in the Y-direction are formed on the lower electrode 44-1.

[0331] The read bit lines RBL1-1, RBL2-1, RBL3-1, and RBL4-1 (write word lines WWL1-1, WWL2-1, WWL3-1, and WWL4-1) are formed on the MTJ elements MTJ1-1, MTJ2-1, MTJ3-1, and MTJ4-1, respectively. The read bit lines RBL1-1, RBL2-1, RBL3-1, and RBL4-1 are in contact with the MTJ elements MTJ1-1, MTJ2-1, MTJ3-1, and MTJ4-1, respectively. The read bit lines RBL1-1, RBL2-1, RBL3-1, and RBL4-1 run in the X-direction (row direction).

[0332] The MTJ elements MTJ1-1, MTJ2-1, MTJ3-1, and MTJ4-1 are independently connected to the read bit lines RBL1-1, RBL2-1, RBL3-1, and RBL4-1, respectively. That is, the four read bit lines RBL1-1, RBL2-1, RBL3-1, and RBL4-1 are arranged in correspondence with the four MTJ elements MTJ1-1, MTJ2-1, MTJ3-1, and MTJ4-1.

[0333] The contact plug 42-1 and conductive layer 43-1 are formed on the lower electrode 44-1. The contact plug 42-1 and conductive layer 43-1 electrically connect the lower electrode 44-1 to the read word line RWL1-1.

[0334] The contact plug 42-1 is arranged at the central portion of the lower electrode 44-1. When the MTJ elements MTJ1-1, MTJ2-1, MTJ3-1, and MTJ4-1 are uniformly arranged to be symmetrical with respect to the contact plug 42-1, signal margin in the read operation due to the interconnection resistance or the like can be maximized.

[0335] The conductive layer 43-1 may be integrated with the contact plug 42-1. More specifically, the conductive layer 43-1 may be omitted, and the contact plug 42-1 may be brought into direct contact with the lower electrode 44-1.

[0336] The read word line RWL1-1 is formed above the MTJ elements MTJ1-1, MTJ2-1, MTJ3-1, and MTJ4-1. The read word line RWL1-1 runs in the Y-direction (column direction).

[2] Second Stage (Memory Cell Array 11-2)

[0337] The read word line RWL1-1 in the memory cell array 11-1 of the first stage also functions as the write bit line WBL1-1 in the memory cell array 11-2 of the second stage.

[0338] More specifically, in the read operation, when the memory cell array 11-1 of the first stage is selected, the read word line/write bit line RWL1-1/WBL1-2 is used as the read word line RWL1-1. In the write operation, when the memory cell array 11-2 of the second stage is selected, the read word line/write bit line RWL1-1/WB1-2 is used as the write bit line WBL1-2.

[0339] A lower electrode 44-2 having, e.g., a rectangular pattern is formed above the write bit line WBL1-2. The four MTJ elements (Magnetic Tunnel Junction elements) MTJ1-2, MTJ2-2, MTJ3-2, and MTJ4-2 arrayed in the Y-direction are formed on the lower electrode 44-2.

[0340] The read bit lines RBL1-2, RBL2-2, RBL3-2, and RBL4-2 (write word lines WWL1-2, WWL2-2, WWL3-2, and WWL4-2) are formed on the MTJ ele-

ments MTJ1-2, MTJ2-2, MTJ3-2, and MTJ4-2, respectively. The read bit lines RBL1-2, RBL2-2, RBL3-2, and RBL4-2 are in contact with the MTJ elements MTJ1-2, MTJ2-2, MTJ3-2, and MTJ4-2, respectively. The read bit lines RBL1-2, RBL2-2, RBL3-2, and RBL4-2 run in the X-direction (row direction).

[0341] The MTJ elements MTJ1-2, MTJ2-2, MTJ3-2, and MTJ4-2 are independently connected to the read bit lines RBL1-2, RBL2-2, RBL3-2, and RBL4-2, respectively. That is, the four read bit lines RBL1-2, RBL2-2, RBL3-2, and RBL4-2 are arranged in correspondence with the four MTJ elements MTJ1-2, MTJ2-2, MTJ3-2, and MTJ4-2.

[0342] The contact plug 42-2 and conductive layer 43-2 are formed on the lower electrode 44-2. The contact plug 42-2 and conductive layer 43-2 electrically connect the lower electrode 44-2 to the read word line RWL1-2.

[0343] The contact plug 42-2 is arranged at the central portion of the lower electrode 44-2. When the MTJ elements MTJ1-2, MTJ2-2, MTJ3-2, and MTJ4-2 are uniformly arranged to be symmetrical with respect to the contact plug 42-2, signal margin in the read operation due to the interconnection resistance or the like can be maximized.

[0344] The conductive layer 43-2 may be integrated with the contact plug 42-2. More specifically, the conductive layer 43-2 may be omitted, and the contact plug 42-2 may be brought into direct contact with the lower electrode 44-2.

[0345] The read word line RWL1-2 is formed above the MTJ elements MTJ1-2, MTJ2-2, MTJ3-2, and MTJ4-2. The read word line RWL1-2 runs in the Y-direction (column direction).

[3] Others

[0346] In the example shown in FIG. 26, the memory cell arrays 11-1 and 11-2 are stacked in two stages on the semiconductor substrate 41. In principle, the memory cell arrays may be stacked in three or more stages (there is no upper limit).

[0347] According to the device structure of Structural Example 4, the memory cell array 11-1 of the lower stage and the memory cell array 11-2 of the upper stage according to Device Structure 2 of Structural Example 2 share one interconnection. For this reason, the density of MTJ elements can be increased. In addition, the underlying layer of the MTJ elements can be planarized (the characteristic of the MTJ elements can be improved).

④ Device Structure (Plan Structure)

[0348] FIGS. 27 to 33 show the layouts of the respective interconnection layers in device structure shown in FIG. 26. The section shown in FIG. 26 corresponds to the section taken along a line XXVI - XXVI in FIGS. 27 to 33.

[0349] FIG. 27 shows the layout of write bit lines of the first stage.

[0350] The write bit lines WBL1-1 run in the Y-direction. The lower electrode 44-1 having a rectangular shape is arranged on each write bit line WBL1-1.

[0351] FIG. 28 shows the layout of MTJ elements of the first stage.

[0352] The MTJ elements MTJ1-1, MTJ2-1, MTJ3-1, and MTJ4-1 and conductive layer 43-1 are arranged on the lower electrode 44-1 having a rectangular pattern.

[0353] The MTJ elements MTJ1-1, MTJ2-1, MTJ3-1, and MTJ4-1 on the lower electrode 44-1 are arranged in the Y-direction. The axis of easy magnetization of the MTJ elements MTJ1-1, MTJ2-1, MTJ3-1, and MTJ4-1, i.e., the direction parallel to the long sides of the MTJ elements MTJ1-1, MTJ2-1, MTJ3-1, and MTJ4-1 is the X-direction.

[0354] FIG. 29 shows the layout of read bit lines of the first stage.

[0355] The read bit lines RBL1-1, RBL2-1, RBL3-1, and RBL4-1 (write word lines WWL1-1, WWL2-1, WWL3-1, and WWL4-1) are arranged on the MTJ elements MTJ1-1, MTJ2-1, MTJ3-1, and MTJ4-1, respectively.

[0356] The read bit lines RBL1-1, RBL2-1, RBL3-1, and RBL4-1 run in the X-direction. The interval between the read bit lines RBL1-1, RBL2-1, RBL3-1, and RBL4-1 can be set to, e.g., the minimum size (or design rule) processible by photolithography.

[0357] The read bit line RBL1-1 is commonly connected to the MTJ elements MTJ1-1 arranged in the X-direction. The read bit line RBL2-1 is commonly connected to the MTJ elements MTJ2-1 arranged in the X-direction. The read bit line RBL3-1 is commonly connected to the MTJ elements MTJ3-1 arranged in the X-direction. The read bit line RBL4-1 is commonly connected to the MTJ elements MTJ4-1 arranged in the X-direction.

[0358] The contact plug 42-1 is arranged on the conductive layer 43-1.

[0359] FIG. 30 shows the layout of read word lines of the first stage/write bit lines of the second stage.

[0360] The read word lines/write bit lines RWL1-1/WBL1-2 run in the Y-direction. The read word line/write bit line RWL1-1/WBL1-2 is in contact with the contact plug 42-1.

[0361] FIG. 31 shows the layout of MTJ elements of the second stage.

[0362] The MTJ elements MTJ1-2, MTJ2-2, MTJ3-2, and MTJ4-2 and conductive layer 43-2 are arranged on the lower electrode 44-2 having a rectangular pattern.

[0363] The MTJ elements MTJ1-2, MTJ2-2, MTJ3-2, and MTJ4-2 on the lower electrode 44-2 are arranged in the Y-direction. The axis of easy magnetization of the MTJ elements MTJ1-2, MTJ2-2, MTJ3-2, and MTJ4-2, i.e., the direction parallel to the long sides of the MTJ elements MTJ1-2, MTJ2-2, MTJ3-2, and MTJ4-2 is the

X-direction.

[0364] FIG. 32 shows the layout of read bit lines of the second stage.

[0365] The read bit lines RBL1-2, RBL2-2, RBL3-2, and RBL4-2 (write word lines WWL1-2, WWL2-2, WWL3-2, and WWL4-2) are arranged on the MTJ elements MTJ1-2, MTJ2-2, MTJ3-2, and MTJ4-2, respectively.

[0366] The read bit lines RBL1-2, RBL2-2, RBL3-2, and RBL4-2 run in the X-direction. The interval between the read bit lines RBL1-2, RBL2-2, RBL3-2, and RBL4-2 can be set to, e.g., the minimum size (or design rule) processible by photolithography.

[0367] The read bit line RBL1-2 is commonly connected to the MTJ elements MTJ1-2 arranged in the X-direction. The read bit line RBL2-2 is commonly connected to the MTJ elements MTJ2-2 arranged in the X-direction. The read bit line RBL3-2 is commonly connected to the MTJ elements MTJ3-2 arranged in the X-direction. The read bit line RBL4-2 is commonly connected to the MTJ elements MTJ4-2 arranged in the X-direction.

[0368] The contact plug 42-2 is arranged on the conductive layer 43-2.

[0369] FIG. 33 shows the layout of read word lines of the second stage.

[0370] The read word lines RWL1-2 run in the Y-direction. The read word line RWL1-2 is in contact with the contact plug 42-2.

(5) Structural Example 5

① Outline

[0371] In Structural Examples 3 and 4, one interconnection is shared as interconnections having different functions of two memory cell arrays (lower and upper stages).

[0372] In Structural Example 5, one interconnection is shared as interconnections having identical functions of two memory cell arrays. When one interconnection is shared as interconnections having identical functions, the switching circuit and disconnecting circuit in Structural Examples 3 and 4 can be omitted. Hence, the peripheral circuit arrangement is simplified.

② Circuit Structure

[0373] In Structural Example 5, in a plurality of stages of memory cell arrays 11-1, 11-2,..., 11-m stacked, the write bit line of the memory cell array of the lower stage and that of the memory cell array of the upper stage are integrated and shared as one write bit line.

[0374] FIGS. 34 and 35 show the main part of a magnetic random access memory according to Structural Example 5 of the present invention.

[1] First Stage (Lower Stage)

[0375] FIG. 34 shows the cell array structure of the first stage of Structural Example 5.

[0376] The memory cell array 11-1 has a plurality of MTJ elements 12 arranged in an array in the X- and Y-directions. For example, j MTJ elements 12 are arranged in the X-direction, and 4 × n MTJ elements 12 are arranged in the Y-direction.

[0377] The four MTJ elements 12 arranged in the Y-direction form one read block BKik (i = 1,..., j, and k = 1,..., n). One row is constructed by j read blocks BKik arranged in the X-direction. The memory cell array 11 has n rows. In addition, one column is constructed by n read blocks BKik arranged in the Y-direction. The memory cell array 11-1 has j columns.

[0378] One terminal of each of the four MTJ elements 12 in the block BKik is commonly connected. The connection point is connected to, e.g., a read word line RWLi-1 (i = 1,..., j). The read word line RWLi-1 runs in the Y-direction. One read word line RWLi-1 is arranged in one column.

[0379] The MTJ elements 12 in the read blocks BKik arranged in one column are directly connected to the read word lines RWLi-1 (i = 1,..., j) without intervening read select switches (MOS transistors). One end of each read word line RWLi-1 is connected to a ground point VSS through a column select switch CSW formed from, e.g., a MOS transistor.

[0380] The column select switches CSW are arranged outside the memory cell array 11-1. Hence, no switch elements (MOS transistors) are arranged in the memory cell array 11-1.

[0381] The other terminal of each of the four MTJ elements 12 in the read block BKik is independently connected to a corresponding one of read bit lines RBL{4(n-1)+1}-1, RBL{4(n-1)+2}-1, RBL{4(n-1)+3}-1, and RBL{4(n-1)+4}-1. That is, the four read bit lines RBL{4(n-1)+1}-1, RBL{4(n-1)+2}-1, RBL{4(n-1)+3}-1, and RBL{4(n-1)+4}-1 are arranged in correspondence with the four MTJ elements 12 in one read block BKik.

[0382] The read bit lines RBL{4(n-1)+1}-1, RBL{4(n-1)+2}-1, RBL{4(n-1)+3}-1, and RBL{4(n-1)+4}-1 run in the X-direction. One end of each read bit line is connected to a common data line 30(1) through a row select switch (MOS transistor) RSW2. The common data line 30(1) is connected to a read circuit 29B(1) (including, e.g., a sense amplifier, selector, and output buffer).

[0383] For example, as shown in FIGS. 116 and 126, the read bit line is connected to a bias transistor BT which sets the bit line potential to VC.

[0384] A row select line signal RLi (i = 1,..., n) is input to each row select switch RSW2. Row decoders 25(1)-1,..., 25(1)-n output the row select line signals RLi.

[0385] As shown in FIG. 116, the bias transistor BT is a PMOS transistor, when the RLi is input to the bias transistor BT. As shown in FIG. 126, the bias transistor BT is a NMOS transistor, when the inverting signal from RLi

is input to the bias transistor BT. Row decoders 25(1)-1,..., 25(1)-n output the row select line signals RLi and the inverting signal thereof.

[0386] The read bit lines RBL{4(n-1)+1}-1, RBL{4(n-1)+2}-1, RBL{4(n-1)+3}-1, and RBL{4(n-1)+4}-1 run in the X-direction and also function as write word lines WWL{4(n-1)+1}-1, WWL{4(n-1)+2}-1, WWL{4(n-1)+3}-1, and WWL{4(n-1)+4}-1, respectively.

[0387] One end of each of the write word lines WWL {4(n-1)+1}-1, WWL{4(n-1)+2}-1, WWL{4(n-1)+3}-1, and WWL{4(n-1)+4}-1 is connected to a write word line driver 23A(1) through the row select switches RSW2 and common data line 30(1). The other end of each write word line is connected to a corresponding one of write word line sinkers 24(1)-1,.., 24(1)-n.

[0388] One write bit line WBLi-1 (i = 1,..., j) which is shared by the four MTJ elements 12 of one read block BKik and run in the Y-direction is arranged near the MTJ elements 12 constituting the read block BKik. One write bit line WBLi-1 is arranged in one column.

[0389] The write bit line WBLi-1 also functions as a write bit line WBLi-2 (i = 1,..., j) in the memory cell array of the second stage.

[0390] Each write bit line WBLi-1 is connected to a circuit block 29A including a column decoder and write bit line driver/sinker. The other end of the write bit line WBLi-1 is connected to a circuit block 31 including a column decoder and write bit line driver/sinker.

[0391] In the write operation, the circuit blocks 29A and 31 are set in an operative state. A write current flows to the write bit lines WBLi-1 in accordance with write data in a direction toward the circuit block 29A or 31.

[0392] In the write operation, the row decoder 25(1)-n selects one of the plurality of rows on the basis of a row address signal. The write word line driver 23A(1) supplies a write current to the write word lines WWL{4(n-1)+1}-1, WWL{4(n-1)+2}-1, WWL{4(n-1)+3}-1, and WWL{4(n-1)+4}-1 in the selected row. The write current is absorbed by the write word line sinker 24(1)-n.

[0393] In read operation, the row decoder 25(1)-n selects one of the plurality of rows on the basis of a row address signal. In the read operation, a column decoder 32(1) selects one of the plurality of columns on the basis of column address signals CSL1,..., CSLj to turn on the column select switch CSW arranged in the selected column.

[2] Second Stage (Upper Stage)

[0394] FIG. 35 shows the cell array structure of the second stage of Structural Example 5.

[0395] The memory cell array 11-2 has the plurality of MTJ elements 12 arranged in an array in the X- and Y-directions. For example, j MTJ elements 12 are arranged in the X-direction, and 4 × n MTJ elements 12 are arranged in the Y-direction.

[0396] The four MTJ elements 12 arranged in the Y-direction form one read block BKik (i = 1,..., j, and k = 1,..., n). One row is constructed by j read blocks BKik arranged in the X-direction. The memory cell array 11 has n rows. In addition, one column is constructed by n read blocks BKik arranged in the Y-direction. The memory cell array 11-2 has j columns.

[0397] One terminal of each of the four MTJ elements 12 in the block BKik is commonly connected. The connection point is connected to, e.g., a read word line RWLi-2 (i = 1,..., j). The read word line RWLi-2 runs in the Y-direction. One read word line RWLi-2 is arranged in one column.

[0398] The MTJ elements 12 in the read blocks BKik arranged in one column are directly connected to the read word lines RWLi-2 (i = 1,..., j) without intervening read select switches (MOS transistors). One end of each read word line RWLi-2 is connected to the ground point VSS through the column select switch CSW formed from a MOS transistor.

[0399] The column select switches CSW are arranged outside the memory cell array 11-2. Hence, no switch elements (MOS transistors) are arranged in the memory cell array 11-2.

[0400] The other terminal of each of the four MTJ elements 12 in the read block BKik is independently connected to a corresponding one of read bit lines RBL{4(n-1)+1}-2, RBL{4(n-1)+2}-2, RBL{4(n-1)+3}-2, and RBL{4(n-1)+4}-2. That is, the four read bit lines RBL{4(n-1)+1}-2, RBL{4(n-1)+2}-2, RBL{4(n-1)+3}-2, and RBL{4(n-1)+4}-2 are arranged in correspondence with the four MTJ elements 12 in one read block BKik.

[0401] The read bit lines RBL{4(n-1)+1}-2, RBL{4(n-1)+2}-2, RBL{4(n-1)+3}-2, and RBL{4(n-1)+4}-2 run in the X-direction. One end of each read bit line is connected to a common data line 30(2) through a row select switch (MOS transistor) RSW2. The common data line 30(2) is connected to a read circuit 29B(2) (including, e.g., a sense amplifier, selector, and output buffer).

[0402] For example, as shown in FIGS. 117 and 127, the read bit line is connected to a bias transistor BT which sets the bit line potential to VC.

[0403] A row select line signal RLi (i = 1,..., n) is input to each row select switch RSW2. Row decoders 25(2)-1,..., 25(2)-n output the row select line signals RLi.

[0404] As shown in FIG. 117, the bias transistor BT is a PMOS transistor, when the RLi is input to the bias transistor BT. As shown in FIG. 127, the bias transistor BT is a NMOS transistor, when the inverting signal from RLi is input to the bias transistor BT. Row decoders 25(2)-1,..., 25(2)-n output the row select line signals RLi and the inverting signal thereof.

[0405] The read bit lines RBL{4(n-1)+1}-2, RBL{4(n-1)+2}-2, RBL{4(n-1)+3}-2, and RBL{4(n-1)+4}-2 run in the X-direction and also function as write word lines WWL{4(n-1)+1}-2, WWL{4(n-1)+2}-2, WWL{4(n-1)+3}-2, and WWL{4(n-1)+4}-2, respectively.

[0406] One end of each of the write word lines WWL {4(n-1)+1}-2, WWL{4(n-1)+2}-2, WWL{4(n-1)+3}-2, and WWL{4(n-1)+4}-2 is connected to a write word line driv-

er 23A(2) through the row select switches RSW2 and common data line 30(2). The other end of each write word line is connected to a corresponding one of write word line sinkers 24(2)-1,.., 24(2)-n.

[0407] One write bit line WBLi-2 (i = 1,..., j) which is shared by the four MTJ elements 12 of one read block BKik and run in the Y-direction is arranged near the MTJ elements 12 constituting the read block BKik. One write bit line WBLi-2 is arranged in one column.

[0408] As described above, the write bit line WBLi-2 is also used as the write bit line WBL1-1 of the memory cell array of the first stage.

[0409] One end of each write bit line WBLi-2 is connected to the circuit block 29A including a column decoder and write bit line driver/sinker. The other end of the write bit line WBLi-2 is connected to the circuit block 31 including a column decoder and write bit line driver/sinker.

[0410] In the write operation, the circuit blocks 29A and 31 are set in an operative state. A write current flows to the write bit lines WBLi-2 in accordance with write data in a direction toward the circuit block 29A or 31.

[0411] In the write operation, the row decoder 25(2)-n selects one of the plurality of rows on the basis of a row address signal. The write word line driver 23A(2) supplies a write current to the write word lines WWL{4(n-1)+1}-2, WWL{4(n-1)+2}-2, WWL{4(n-1)+3}-2, and WWL{4(n-1)+4}-2 in the selected row. The write current is absorbed by the write word line sinker 24(2)-n.

[0412] In the read operation, the row decoder 25(2)-n selects one of the plurality of rows on the basis of a row address signal. In the read operation, a column decoder 32(2) selects one of the plurality of columns on the basis of column address signals CSL1,..., CSLj to turn on the column select switch CSW arranged in the selected column.

③ Device Structure (Sectional Structure)

[0413] As a characteristic feature of the device structure of Structural Example 5, Device Structure 2 (FIG. 4) of Structural Example 1 is employed for the memory cell array of the first stage, Device Structure 3 (FIG. 8) of Structural Example 1 is employed for the memory cell array of the second stage, and the write bit line is shared.

[0414] FIG. 36 shows a device structure corresponding to one block of the magnetic random access memory according to Structural Example 5 of the present invention.

[1] First Stage (Memory Cell Array 11-1)

[0415] A read word line RWL1-1 running in the Y-direction is formed on a semiconductor substrate 41. No switch element is arranged immediately under the read word line RWL1-1. Four MTJ elements (Magnetic Tunnel Junction elements) MTJ1-1, MTJ2-1, MTJ3-1, and MTJ4-1 arrayed in the Y-direction are formed above the read word line RWL1-1.

[0416] One terminal (upper end in this example) of each of the MTJ elements MTJ1-1, MTJ2-1, MTJ3-1, and MTJ4-1 is commonly connected to an upper electrode 44-1. A contact plug 42-1 and conductive layer 43-1 electrically connect the upper electrode 44-1 to the read word line RWL1-1.

[0417] The contact plug 42-1 is arranged at the central portion of the upper electrode 44-1. When the MTJ elements MTJ1-1, MTJ2-1, MTJ3-1, and MTJ4-1 are uniformly arranged to be symmetrical with respect to the contact plug 42-1, signal margin in the read operation due to the interconnection resistance or the like can be maximized.

[0418] The conductive layer 43-1 may be integrated with the upper electrode 44-1. That is, the conductive layer 43-1 and upper electrode 44-1 may be formed simultaneously using the same material.

[0419] The other terminal (lower end in this example) of each of the MTJ elements MTJ1-1, MTJ2-1, MTJ3-1, and MTJ4-1 is electrically connected to a corresponding one of read bit lines RBL1-1, RBL2-1, RBL3-1, and RBL4-1 (write word lines WWL1-1, WWL2-1, WWL3-1, and WWL4-1). The read bit lines RBL1-1, RBL2-1, RBL3-1, and RBL4-1 run in the X-direction (row direction).

[0420] The MTJ elements MTJ1-1, MTJ2-1, MTJ3-1, and MTJ4-1 are independently connected to the read bit lines RBL1-1, RBL2-1, RBL3-1, and RBL4-1, respectively. That is, the four read bit lines RBL1-1, RBL2-1, RBL3-1, and RBL4-1 are arranged in correspondence with the four MTJ elements MTJ1-1, MTJ2-1, MTJ3-1, and MTJ4-1.

[0421] A write bit line WBL1-1 is formed above and near the MTJ elements MTJ1-1, MTJ2-1, MTJ3-1, and MTJ4-1. The write bit line WBL1-1 runs in the Y-direction (column direction).

[2] Second Stage (Memory Cell Array 11-2)

[0422] A write bit line WBL1-1 in the memory cell array 11-1 of the first stage also functions as a write bit line WBL1-2 in the memory cell array 11-2 of the second stage.

[0423] More specifically, in write operation, when the memory cell array 11-1 of the first stage is selected, and the memory cell array 11-2 of the second stage is selected, a write current flows to the write bit line WBL1-1/WBL1-2.

[0424] Four MTJ elements (Magnetic Tunnel Junction elements) MTJ1-2, MTJ2-2, MTJ3-2, and MTJ4-2 arrayed in the Y-direction are formed above the write bit line WBL1-2.

[0425] One terminal (lower end in this example) of each of the MTJ elements MTJ1-2, MTJ2-2, MTJ3-2, and MTJ4-2 is commonly connected to a lower electrode 44-2. A contact plug 42-2 and conductive layer 43-2 electrically connect the lower electrode 44-2 to the

read word line RWL1-2.

[0426] The contact plug 42-2 is arranged at the central portion of the lower electrode 44-2. When the MTJ elements MTJ1-2, MTJ2-2, MTJ3-2, and MTJ4-2 are uniformly arranged to be symmetrical with respect to the contact plug 42-2, signal margin in the read operation due to the interconnection resistance or the like can be maximized.

[0427] The conductive layer 43-2 may be integrated with contact plug 42-2. More specifically, the conductive layer 43-2 may be omitted, and the contact plug 42-2 may be brought into direct contact with the lower electrode 44-2.

[0428] The other terminal (upper end in this example) of each of the MTJ elements MTJ1-2, MTJ2-2, MTJ3-2, and MTJ4-2 is electrically connected to a corresponding one of read bit lines RBL1-2, RBL2-2, RBL3-2, and RBL4-2 (write word lines WWL1-2, WWL2-2, WWL3-2, and WWL4-2). The read bit lines RBL1-2, RBL2-2, RBL3-2, and RBL4-2 run in the X-direction (row direction).

[0429] The MTJ elements MTJ1-2, MTJ2-2, MTJ3-2, and MTJ4-2 are independently connected to the read bit lines RBL1-2, RBL2-2, RBL3-2, and RBL4-2, respectively. That is, the four read bit lines RBL1-2, RBL2-2, RBL3-2, and RBL4-2 are arranged in correspondence with the four MTJ elements MTJ1-2, MTJ2-2, MTJ3-2, and MTJ4-2.

[0430] A write bit line WBL1-2 is formed above and near the MTJ elements MTJ1-2, MTJ2-2, MTJ3-2, and MTJ4-2. The write bit line WBL1-2 runs in the Y-direction (column direction).

[3] Others

[0431] In the example shown in FIG. 36, the memory cell arrays 11-1 and 11-2 are stacked in two stages on the semiconductor substrate 41. In principle, the memory cell arrays may be stacked in 2 × a (a is a natural number) stages. The memory cell arrays may be stacked in three or more stages (there is no upper limit) by combining Structural Example 5 and Structural Example 6 (to be described later).

[0432] According to the device structure of Structural Example 5, the memory cell array 11-1 of the lower stage and the memory cell array 11-2 of the upper stage share one interconnection. For this reason, the degree of integration of MTJ elements can be increased, and the underlying layer of the MTJ elements can be planarized (the characteristic of the MTJ elements can be improved).

④ Device Structure (Plane Structure)

[0433] FIGS. 37 to 43 show the layouts of the respective interconnection layers in the device structure shown in FIG. 36. The section shown in FIG. 36 corresponds to the section taken along a line XXXVI - XXXVI in FIGS. 37 to 43.

[0434] FIG. 37 shows the layout of read word lines of the first stage.

[0435] The read word lines RWL1-1 run in the Y-direction. The contact plug 42-1 is arranged on each read word line RWL1-1.

[0436] FIG. 38 shows the layout of read bit lines of the first stage and MTJ elements of the first stage.

[0437] The read bit lines RBL1-1, RBL2-1, RBL3-1, and RBL4-1 (write word lines WWL1-1, WWL2-1, WWL3-1, and WWL4-1) run in the X-direction. The interval between the read bit lines RBL1-1, RBL2-1, RBL3-1, and RBL4-1 can be set to, e.g., the minimum size (or design rule) processible by photolithography.

[0438] The MTJ elements MTJ1-1, MTJ2-1, MTJ3-1, and MTJ4-1 are arranged on the read bit lines RBL1-1, RBL2-1, RBL3-1, and RBL4-1. The axis of easy magnetization of the MTJ elements MTJ1-1, MTJ2-1, MTJ3-1, and MTJ4-1, i.e., the direction parallel to the long sides of the MTJ elements MTJ1-1, MTJ2-1, MTJ3-1, and MTJ4-1 is the X-direction.

[0439] The read bit line RBL1-1 is commonly connected to the MTJ elements MTJ1-1 arranged in the X-direction. The read bit line RBL2-1 is commonly connected to the MTJ elements MTJ2-1 arranged in the X-direction. The read bit line RBL3-1 is commonly connected to the MTJ elements MTJ3-1 arranged in the X-direction. The read bit line RBL4-1 is commonly connected to the MTJ elements MTJ4-1 arranged in the X-direction.

[0440] The conductive layer 43-1 is arranged on the contact plug 42-1.

[0441] FIG. 39 shows the layout of write bit lines of the first stage/write bit lines of the second stage.

[0442] The upper electrodes 44-1 each having a rectangular pattern are arranged on the MTJ elements MTJ1-1, MTJ2-1, MTJ3-1, and MTJ4-1 and conductive layers 43. The upper electrodes 44-1 are in contact with the MTJ elements MTJ1-1, MTJ2-1, MTJ3-1, and MTJ4-1 and conductive layers 43-1.

[0443] The write bit lines WBL1-1/WBL1-2 are arranged immediately on the upper electrodes 44-1. The write bit lines WBL1-1/WBL1-2 run in the Y-direction.

[0444] FIG. 40 shows the layout of lower electrodes of the second stage.

[0445] The lower electrodes 44-2 each having a rectangular pattern are arranged on the write bit lines WBL1-1/WBL1-2. The upper electrodes 44-1 and lower electrodes 44-2 may be arranged to be symmetrical with respect to the write bit lines WBL1-1/WBL1-2, as in this example, or may be arranged asymmetrically.

[0446] FIG. 41 shows the layout of MTJ elements of the second stage.

[0447] The MTJ elements MTJ1-2, MTJ2-2, MTJ3-2, and MTJ4-2 and conductive layers 43-2 are arranged on the lower electrodes 44-2 each having a rectangular pattern.

[0448] The MTJ elements MTJ1-2, MTJ2-2, MTJ3-2,

and MTJ4-2 on the lower electrodes 44-2 are arranged in the Y-direction. The axis of easy magnetization of the MTJ elements MTJ1-2, MTJ2-2, MTJ3-2, and MTJ4-2, i.e., the direction parallel to the long sides of the MTJ elements MTJ1-2, MTJ2-2, MTJ3-2, and MTJ4-2 is the X-direction.

[0449] FIG. 42 shows the layout of read word lines of second stage.

[0450] The read bit lines RBL1-2, RBL2-2, RBL3-2, and RBL4-2 (write word lines WWL1-2, WWL2-2, WWL3-2, and WWL4-2) are arranged on the MTJ elements MTJ1-2, MTJ2-2, MTJ3-2, and MTJ4-2, respectively.

[0451] The read bit lines RBL1-2, RBL2-2, RBL3-2, and RBL4-2 run in the X-direction. The interval between the read bit lines RBL1-2, RBL2-2, RBL3-2, and RBL4-2 can be set to, e.g., the minimum size (or design rule) processible by photolithography.

[0452] The read bit line RBL1-2 is commonly connected to the MTJ elements MTJ1-2 arranged in the X-direction. The read bit line RBL2-2 is commonly connected to the MTJ elements MTJ2-2 arranged in the X-direction. The read bit line RBL3-2 is commonly connected to the MTJ elements MTJ3-2 arranged in the X-direction. The read bit line RBL4-2 is commonly connected to the MTJ elements MTJ4-2 arranged in the X-direction.

[0453] The contact plug 42-2 is arranged on the conductive layer 43-2.

[0454] FIG. 43 shows the layout of read word lines of the second stage.

[0455] The read word lines RWL1-2 run in the Y-direction. The read word line RWL1-2 is in contact with the contact plug 42-2.

(6) Structural Example 6

① Outline

[0456] In Structural Example 6, one interconnection is shared as interconnections having identical functions of two memory cell arrays, like Structural Example 5. In Structural Example 5, a write bit line is shared. However, in Structural Example 6, a read word line is shared.

[0457] When one interconnection is shared as interconnections having identical functions, the switching circuit and disconnecting circuit in Structural Examples 3 and 4 can be omitted. Hence, the peripheral circuit arrangement is simplified.

② Circuit Structure

[0458] In Structural Example 6, in a plurality of stages of memory cell arrays 11-1, 11-2,..., 11-m stacked, the read word line of the memory cell array of the lower stage and that of the memory cell array of the upper stage are integrated and shared as one read word line.

[0459] FIGS. 44 and 45 show the main part of a magnetic random access memory according to Structural Example 6 of the present invention.

[1] First Stage (Lower Stage)

[0460] FIG. 44 shows the cell array structure of the first stage of Structural Example 6.

[0461] The memory cell array 11-1 has a plurality of MTJ elements 12 arranged in an array in the X- and Y-directions. For example, j MTJ elements 12 are arranged in the X-direction, and 4 × n MTJ elements 12 are arranged in the Y-direction.

[0462] The four MTJ elements 12 arranged in the Y-direction form one read block BKik (i = 1,..., j, and k = 1,..., n). One row is constructed by j read blocks BKik arranged in the X-direction. The memory cell array 11 has n rows. In addition, one column is constructed by n read blocks BKik arranged in the Y-direction. The memory cell array 11-1 has j columns.

[0463] One terminal of each of the four MTJ elements 12 in the block BKik is commonly connected. The connection point is connected to, e.g., a read word line RWLi-1 (i = 1,..., j). The read word line RWLi-1 also functions as a read word line RWLi-2 of the memory cell array of the second stage (to be described later). The read word line RWLi-1 runs in the Y-direction. One read word line RWLi-1 is arranged in one column.

[0464] The MTJ elements 12 in the read blocks BKik arranged in one column are directly connected to the read word lines RWLi-1 (i = 1,..., j) without intervening read select switches (MOS transistors). One end of each read word line RWLi-1 is connected to a ground point VSS through a column select switch CSW formed from a MOS transistor.

[0465] The column select switches CSW are arranged outside the memory cell array 11-1. Hence, no switch elements (MOS transistors) are arranged in the memory cell array 11-1.

[0466] The other terminal of each of the four MTJ elements 12 in the read block BKik is independently connected to a corresponding one of read bit lines RBL{4(n-1)+1}-1, RBL{4(n-1)+2}-1, RBL{4(n-1)+3}-1, and RBL{4(n-1)+4}-1. That is, the four read bit lines RBL{4(n-1)+1}-1, RBL{4(n-1)+2}-1, RBL{4(n-1)+3}-1, and RBL{4(n-1)+4}-1 are arranged in correspondence with the four MTJ elements 12 in one read block BKik.

[0467] The read bit lines RBL{4(n-1)+1}-1, RBL{4(n-1)+2}-1, RBL{4(n-1)+3}-1, and RBL{4(n-1)+4}-1 run in the X-direction. One end of each read bit line is connected to a common data line 30(1) through a row select switch (MOS transistor) RSW2. The common data line 30(1) is connected to a read circuit 29B(1) (including, e.g., a sense amplifier, selector, and output buffer).

[0468] For example, as shown in FIGS. 118 and 128, the read bit line is connected to a bias transistor BT which sets the bit line potential to VC.

[0469] A row select line signal RLi (i = 1,..., n) is input to each row select switch RSW2. Row decoders 25(1)-

1,..., 25(1)-n output the row select line signals RLi.

[0470] As shown in FIG. 118, the bias transistor BT is a PMOS transistor, when the RLi is input to the bias transistor BT. As shown in FIG. 128, the bias transistor BT is a NMOS transistor, when the inverting signal from RLi is input to the bias transistor BT. Row decoders 25(1)-1,..., 25(1)-n output the row select line signals RLi and the inverting signal thereof.

[0471] The read bit lines RBL{4(n-1)+1}-1, RBL{4(n-1)+2}-1, RBL{4(n-1)+3}-1, and RBL{4(n-1)+4}-1 run in the X-direction and also function as write word lines WWL{4(n-1)+1}-1, WWL{4(n-1)+2}-1, WWL{4(n-1)+3}-1, and WWL{4(n-1)+4}-1, respectively.

[0472] One end of each of the write word lines WWL {4(n-1)+1}-1, WWL{4(n-1)+2}-1, WWL{4(n-1)+3}-1, and WWL{4(n-1)+4}-1 is connected to a write word line driver 23A(1) through the row select switches RSW2 and common data line 30(1). The other end of each write word line is connected to a corresponding one of write word line sinkers 24(1)-1, .., 24(1)-n.

[0473] One write bit line WBLi-1 (i = 1,..., j) which is shared by the four MTJ elements 12 of one read block BKik and run in the Y-direction is arranged near the MTJ elements 12 constituting the read block BKik. One write bit line WBLi-1 is arranged in one column.

[0474] One end of each write bit line WBLi-1 is connected to a circuit block 29A(1) including a column decoder and write bit line driver/sinker. The other end of the write bit line WBLi-1 is connected to a circuit block 31(1) including a column decoder and write bit line driver/sinker.

[0475] In the write operation, the circuit blocks 29A(1) and 31(1) are set in an operative state. A write current flows to the write bit lines WBLi-2 in accordance with write data in a direction toward the circuit block 29A(1) or 31(1).

[0476] In the write operation, the row decoder 25(1)-n selects one of the plurality of rows on the basis of a row address signal. The write word line driver 23A(1) supplies a write current to the write word lines WWL{4(n-1)+1}-1, WWL{4(n-1)+2}-1, WWL{4(n-1)+3}-1, and WWL{4(n-1)+4}-1 in the selected row. The write current is absorbed by the write word line sinker 24(1)-n.

[0477] In read operation, the row decoder 25(1)-n selects one of the plurality of rows on the basis of a row address signal. In the read operation, a column decoder 32 selects one of the plurality of columns on the basis of column address signals CSL1,..., CSLj to turn on the column select switch CSW arranged in the selected column.

[2] Second Stage (Upper Stage)

[0478] FIG. 45 shows the cell array structure of the second stage of Structural Example 6.

[0479] The memory cell array 11-2 has the plurality of MTJ elements 12 arranged in an array in the X- and Y-directions. For example, j MTJ elements 12 are arranged in the X-direction, and 4 × n MTJ elements 12 are arranged in the Y-direction.

[0480] The four MTJ elements 12 arranged in the Y-direction form one read block BKik (i = 1,..., j, and k = 1,..., n). One row is constructed by j read blocks BKik arranged in the X-direction. The memory cell array 11 has n rows. In addition, one column is constructed by n read blocks BKik arranged in the Y-direction. The memory cell array 11-2 has j columns.

[0481] One terminal of each of the four MTJ elements 12 in the block BKik is commonly connected. The connection point is connected to, e.g., a read word line RWLi-2 (i = 1,..., j). The read word line RWLi-2 also functions as the read word line RWLi-1 of the memory cell array of the first stage. The read word line RWLi-2 runs in the Y-direction. One read word line RWLi-2 is arranged in one column.

[0482] The MTJ elements 12 in the read blocks BKik arranged in one column are directly connected to the read word lines RWLi-2 (i = 1,..., j) without intervening read select switches (MOS transistors). One end of each read word line RWLi-2 is connected to the ground point VSS through the column select switch CSW formed from, e.g., a MOS transistor.

[0483] The other terminal of each of the four MTJ elements 12 in the read block BKik is independently connected to a corresponding one of read bit lines RBL{4(n-1)+1}-2, RBL{4(n-1)+2}-2, RBL{4(n-1)+3}-2, and RBL{4(n-1)+4}-2. That is, the four read bit lines RBL{4(n-1)+1}-2, RBL{4(n-1)+2}-2, RBL{4(n-1)+3}-2, and RBL{4(n-1)+4}-2 are arranged in correspondence with the four MTJ elements 12 in one read block BKik.

[0484] The read bit lines RBL{4(n-1)+1}-2, RBL{4(n-1)+2}-2, RBL{4(n-1)+3}-2, and RBL{4(n-1)+4}-2 run in the X-direction. One end of each read bit line is connected to a common data line 30(2) through a row select switch (MOS transistor) RSW2. The common data line 30(2) is connected to a read circuit 29B(2) (including, e.g., a sense amplifier, selector, and output buffer).

[0485] For example, as shown in FIGS. 119 and 129, the read bit line is connected to a bias transistor BT which sets the bit line potential to VC.

[0486] A row select line signal RLi (i = 1,..., n) is input to each row select switch RSW2. Row decoders 25(2)-1,..., 25(2)-n output the row select line signals RLi.

[0487] As shown in FIG. 119, the bias transistor BT is a PMOS transistor, when the RLi is input to the bias transistor BT. As shown in FIG. 129, the bias transistor BT is a NMOS transistor, when the inverting signal from RLi is input to the bias transistor BT. Row decoders 25(2)-1,..., 25(2)-n output the row select line signals RLi and the inverting signal thereof.

[0488] The read bit lines RBL{4(n-1)+1}-2, RBL{4(n-1)+2}-2, RBL{4(n-1)+3}-2, and RBL{4(n-1)+4}-2 run in the X-direction and also function as write word lines WWL{4(n-1)+1}-2, WWL{4(n-1)+2}-2, WWL{4(n-1)+3}-2, and WWL{4(n-1)+4}-2, respectively.

[0489] One end of each of the write word lines WWL

{4(n-1)+1}-2, WWL{4(n-1)+2}-2, WWL{4(n-1)+3}-2, and WWL{4(n-1)+4}-2 is connected to a write word line driver 23A(2) through the row select switches RSW2 and common data line 30(2). The other end of each write word line is connected to a corresponding one of write word line sinkers 24(2)-1,.., 24(2)-n.

[0490] One write bit line WBLi-2 (i = 1,..., j) which is shared by the four MTJ elements 12 of one read block BKik and run in the Y-direction is arranged near the MTJ elements 12 constituting the read block BKik. One write bit line WBLi-2 is arranged in one column.

[0491] One end of each write bit line WBLi-2 is connected to a circuit block 29A(2) including a column decoder and write bit line driver/sinker. The other end of the write bit line WBLi-2 is connected to a circuit block 31(2) including a column decoder and write bit line driver/sinker.

[0492] In the write operation, the circuit blocks 29A(2) and 31(2) are set in an operative state. A write current flows to the write bit lines WBLi-2 in accordance with write data in a direction toward the circuit block 29A(2) or 31(2).

[0493] In the write operation, the row decoder 25(2)-n selects one of the plurality of rows on the basis of a row address signal. The write word line driver 23A(2) supplies a write current to the write word lines WWL{4(n-1)+1}-2, WWL{4(n-1)+2}-2, WWL{4(n-1)+3}-2, and WWL{4(n-1)+4}-2 in the selected row. The write current is absorbed by the write word line sinker 24(2)-n.

[0494] In the read operation, the row decoder 25(2)-n selects one of the plurality of rows on the basis of a row address signal. In the read operation, a column decoder 32 selects one of the plurality of columns on the basis of column address signals CSL1,..., CSLj to turn on the column select switch CSW arranged in the selected column.

③ Device Structure (Sectional Structure)

[0495] As a characteristic feature of the device structure of Structural Example 6, Device Structure 3 (FIG. 8) of Structural Example 1 is employed for the memory cell array of the first stage, Device Structure 2 (FIG. 4) of Structural Example 1 is employed for the memory cell array of the second stage, and the read word line is shared.

[0496] FIG. 46 shows a device structure corresponding to one block of the magnetic random access memory according to Structural Example 6 of the present invention.

[1] First Stage (Memory Cell Array 11-1)

[0497] The write bit line WBL1-1 running in the Y-direction is formed on a semiconductor substrate 41. No switch element is arranged immediately under the write bit line WBL1-1. A lower electrode 44-1 having, e.g., a rectangular pattern is formed above the write bit line WBL1-1.

[0498] The four MTJ elements (Magnetic Tunnel Junction elements) MTJ1-1, MTJ2-1, MTJ3-1, and MTJ4-1 arrayed in the Y-direction are formed on the lower electrode 44-1.

[0499] The read bit lines RBL1-1, RBL2-1, RBL3-1, and RBL4-1 (write word lines WWL1-1, WWL2-1, WWL3-1, and WWL4-1) are formed on the MTJ elements MTJ1-1, MTJ2-1, MTJ3-1, and MTJ4-1, respectively. The read bit lines RBL1-1, RBL2-1, RBL3-1, and RBL4-1 are in contact with the MTJ elements MTJ1-1, MTJ2-1, MTJ3-1, and MTJ4-1, respectively. The read bit lines RBL1-1, RBL2-1, RBL3-1, and RBL4-1 run in the X-direction (row direction).

[0500] The MTJ elements MTJ1-1, MTJ2-1, MTJ3-1, and MTJ4-1 are independently connected to the read bit lines RBL1-1, RBL2-1, RBL3-1, and RBL4-1, respectively. That is, the four read bit lines RBL1-1, RBL2-1, RBL3-1, and RBL4-1 are arranged in correspondence with the four MTJ elements MTJ1-1, MTJ2-1, MTJ3-1, and MTJ4-1.

[0501] A contact plug 42-1 and conductive layer 43-1 are formed on the lower electrode 44-1. The contact plug 42-1 and conductive layer 43-1 electrically connect the lower electrode 44-1 to the read word line RWL1-1.

[0502] The contact plug 42-1 is arranged at the central portion of the lower electrode 44-1. When the MTJ elements MTJ1-1, MTJ2-1, MTJ3-1, and MTJ4-1 are uniformly arranged to be symmetrical with respect to the contact plug 42-1, signal margin in the read operation due to the interconnection resistance or the like can be maximized.

[0503] The read word line RWL1-1 is formed above the MTJ elements MTJ1-1, MTJ2-1, MTJ3-1, and MTJ4-1. The read word line RWL1-1 runs in the Y-direction (column direction).

[2] Second Stage (Memory Cell Array 11-2)

[0504] The read word line RWL1-1 in the memory cell array 11-1 of the first stage also functions as the read word line RWL1-2 in the memory cell array 11-2 of the second stage.

[0505] More specifically, in the read operation, when the memory cell array 11-1 of the first stage is selected, and the memory cell array 11-2 of the second stage is selected, the read word line RWL1-1/RWL1-2 is short-circuited to the ground point.

[0506] An upper electrode 44-2 having, e.g., a rectangular pattern is formed above the read word line RWL1-2. The four MTJ elements (Magnetic Tunnel Junction elements) MTJ1-2, MTJ2-2, MTJ3-2, and MTJ4-2 arrayed in the Y-direction are formed immediately under the upper electrode 44-2.

[0507] The read bit lines RBL1-2, RBL2-2, RBL3-2, and RBL4-2 (write word lines WWL1-2, WWL2-2, WWL3-2, and WWL4-2) are formed immediately under the MTJ elements MTJ1-2, MTJ2-2, MTJ3-2, and

MTJ4-2, respectively. The read bit lines RBL1-2, RBL2-2, RBL3-2, and RBL4-2 are in contact with the MTJ elements MTJ1-2, MTJ2-2, MTJ3-2, and MTJ4-2, respectively. The read bit lines RBL1-2, RBL2-2, RBL3-2, and RBL4-2 run in the X-direction (row direction).

[0508] The MTJ elements MTJ1-2, MTJ2-2, MTJ3-2, and MTJ4-2 are independently connected to the read bit lines RBL1-2, RBL2-2, RBL3-2, and RBL4-2, respectively. That is, the four read bit lines RBL1-2, RBL2-2, RBL3-2, and RBL4-2 are arranged in correspondence with the four MTJ elements MTJ1-2, MTJ2-2, MTJ3-2, and MTJ4-2.

[0509] A contact plug 42-2 and conductive layer 43-2 are formed between the upper electrode 44-2 and the read word line RWL1-2. The contact plug 42-2 and conductive layer 43-2 electrically connect the upper electrode 44-2 to the read word line RWL1-2.

[0510] The contact plug 42-2 is arranged at the central portion of the upper electrode 44-2. When the MTJ elements MTJ1-2, MTJ2-2, MTJ3-2, and MTJ4-2 are uniformly arranged to be symmetrical with respect to the contact plug 42-2, signal margin in the read operation due to the interconnection resistance or the like can be maximized.

[0511] The write bit line WBL1-2 is formed above the MTJ elements MTJ1-2, MTJ2-2, MTJ3-2, and MTJ4-2. The write bit line WBL1-2 runs in the Y-direction (column direction).

[3] Others

[0512] In the example shown in FIG. 46, the memory cell arrays 11-1 and 11-2 are stacked in two stages on the semiconductor substrate 41. In principle, the memory cell arrays may be stacked in $2 \times a$ (a is a natural number) stages. The memory cell arrays may be stacked in three or more stages (there is no upper limit) by combining Structural Examples 5 and 6.

[0513] According to the device structure of Structural Example 6, the memory cell array 11-1 of the lower stage and the memory cell array 11-2 of the upper stage share one interconnection. For this reason, the degree of integration of MTJ elements can be increased, and the underlying layer of the MTJ elements can be planarized (the characteristic of the MTJ elements can be improved).

④ Device Structure (Plan Structure)

[0514] FIGS. 47 to 52 show the layouts of the respective interconnection layers in device structure shown in FIG. 46. The section shown in FIG. 46 corresponds to the section taken along a line XLVI - XLVI in FIGS. 47 to 52.

[0515] FIG. 47 shows the layout of write bit lines of the first stage.

[0516] The write bit lines WBL1-1 run in the Y-direction. The lower electrode 44-1 having a rectangular shape is arranged on each write bit line WBL1-1.

[0517] FIG. 48 shows the layout of MTJ elements of the first stage.

[0518] The MTJ elements MTJ1-1, MTJ2-1, MTJ3-1, and MTJ4-1 and conductive layer 43-1 are arranged on the lower electrode 44-1 having a rectangular pattern.

[0519] The MTJ elements MTJ1-1, MTJ2-1, MTJ3-1, and MTJ4-1 on the lower electrode 44-1 are arranged in the Y-direction. The axis of easy magnetization of the MTJ elements MTJ1-1, MTJ2-1, MTJ3-1, and MTJ4-1, i.e., the direction parallel to the long sides of the MTJ elements MTJ1-1, MTJ2-1, MTJ3-1, and MTJ4-1 is the X-direction.

[0520] FIG. 49 shows the layout of read bit lines of the first stage.

[0521] The read bit lines RBL1-1, RBL2-1, RBL3-1, and RBL4-1 (write word lines WWL1-1, WWL2-1, WWL3-1, and WWL4-1) are arranged on the MTJ elements MTJ1-1, MTJ2-1, MTJ3-1, and MTJ4-1, respectively.

[0522] The read bit lines RBL1-1, RBL2-1, RBL3-1, and RBL4-1 run in the X-direction. The interval between the read bit lines RBL1-1, RBL2-1, RBL3-1, and RBL4-1 can be set to, e.g., the minimum size (or design rule) processible by photolithography.

[0523] The read bit line RBL1-1 is commonly connected to the MTJ elements MTJ1-1 arranged in the X-direction. The read bit line RBL2-1 is commonly connected to the MTJ elements MTJ2-1 arranged in the X-direction. The read bit line RBL3-1 is commonly connected to the MTJ elements MTJ3-1 arranged in the X-direction. The read bit line RBL4-1 is commonly connected to the MTJ elements MTJ4-1 arranged in the X-direction.

[0524] The contact plug 42-1 is arranged on the conductive layer 43-1.

[0525] FIG. 50 shows the layout of read word lines of the first stage/read word lines of the second stage.

[0526] The read word lines RWL1-1/RWL1-2 run in the Y-direction. The read word line RWL1-1/RWL1-2 is in contact with the contact plug 42-1. The contact plug 42-2 is formed on the read word line RWL1-1/RWL1-2.

[0527] FIG. 51 shows the layout of read bit lines of the second stage and MTJ elements of the second stage.

[0528] The read bit lines RBL1-2, RBL2-2, RBL3-2, and RBL4-2 (write word lines WWL1-2, WWL2-2, WWL3-2, and WWL4-2) run in the X-direction. The interval between the read bit lines RBL1-2, RBL2-2, RBL3-2, and RBL4-2 can be set to, e.g., the minimum size (or design rule) processible by photolithography.

[0529] The MTJ elements MTJ1-2, MTJ2-2, MTJ3-2, and MTJ4-2 are arranged on the read bit lines RBL1-2, RBL2-2, RBL3-2, and RBL4-2. The axis of easy magnetization of the MTJ elements MTJ1-2, MTJ2-2, MTJ3-2, and MTJ4-2, i.e., the direction parallel to the long sides of the MTJ elements MTJ1-2, MTJ2-2, MTJ3-2, and MTJ4-2 is the X-direction.

[0530] The read bit line RBL1-2 is commonly connected to the MTJ elements MTJ1-2 arranged in the X-direction. The read bit line RBL2-2 is commonly connected to the MTJ elements MTJ2-2 arranged in the X-direction. The read bit line RBL3-2 is commonly connected to the MTJ elements MTJ3-2 arranged in the X-direction. The read bit line RBL4-2 is commonly connected to the MTJ elements MTJ4-2 arranged in the X-direction.

[0531] The conductive layer 43-2 is arranged on the contact plug 42-2.

[0532] FIG. 52 shows the layout of write bit lines of the second stage.

[0533] The upper electrodes 44-2 each having a rectangular pattern are arranged on the MTJ elements MTJ1-2, MTJ2-2, MTJ3-2, and MTJ4-2 and conductive layer 43-2. The upper electrodes 44-2 are in contact with the MTJ elements MTJ1-2, MTJ2-2, MTJ3-2, and MTJ4-2 and conductive layers 43-2.

[0534] The write bit lines WBL1-2 are arranged immediately on the upper electrodes 44-2. The write bit lines WBL1-2 run in the Y-direction.

(7) Structural Example 7

[0535] Structural Example 7 is a modification of Structural Example 1. As its characteristic feature, the axis of easy magnetization of the MTJ element of Structural Example 1 is rotated by 90°.

[0536] In Structural Example 1, the axis of easy magnetization of the MTJ element is the X-direction (row direction), and the axis of hard magnetization is the Y-direction (column direction). That is, the MTJ element has a rectangular shape long in the X-direction. To the contrary, in Structural Example 7, the axis of easy magnetization of the MTJ element is the Y-direction, and the axis of hard magnetization is the X-direction. That is, the MTJ element has a rectangular shape long in the Y-direction.

[0537] In a magnetic random access memory, basically, data is written in a memory cell (the direction of magnetization of the pinning layer is determined) by changing the direction of a write current flowing to a write line that runs in a direction parallel to the axis of hard magnetization.

[0538] Hence, in this example, data to be written in a memory cell is determined by controlling the direction of a write current flowing to a write bit line (read bit line) that runs in the X-direction in write operation.

[0539]. Generally, a write line that runs along the axis of hard magnetization (in a direction parallel to the short axis of an MTJ) is called a write bit line.

① Circuit Structure

[0540] FIG. 53 shows the main part of a magnetic random access memory according to Structural Example 7 of the present invention.

[0541] A memory cell array 11 has a plurality of MTJ elements 12 arranged in an array in the X- and Y-directions. For example, j MTJ elements 12 are arranged in the X-direction, and 4 × n MTJ elements 12 are arranged in the Y-direction.

[0542] The four MTJ elements 12 arranged in the Y-direction form one read block BKik (i = 1,..., j, and k = 1,..., n). One row is constructed by j read blocks BKik arranged in the X-direction. The memory cell array 11 has n rows. In addition, one column is constructed by n read blocks BKik arranged in the Y-direction. The memory cell array 11 has j columns.

[0543] One terminal of each of the four MTJ elements 12 in the block BKik is commonly connected. The connection point is directly connected to a read word line RWLi (i = 1,..., j) without intervening read select switches. The read word line RWLi runs in the Y-direction. One read word line RWLi is arranged in one column.

[0544] Each read word line RWLi is connected to a ground point VSS through a column select switch CSW formed from, e.g., a MOS transistor.

[0545] In read operation, in a selected row, a row select switch RSW2 is turned on. In a selected column, the column select switch CSW is turned on. For this reason, the potential of the read word line RWLi becomes the ground potential VSS. A read current flows to the MTJ elements 12 in the read block BKik located at the intersection between the selected row and the selected column.

[0546] The other terminal of each of the four MTJ elements 12 in the read block BKik is independently connected to a corresponding one of read bit lines RBL4(n-1)+1, RBL4(n-1)+2, RBL4(n-1)+3, and RBL4(n-1)+4. That is, the four read bit lines RBL4(n-1)+1, RBL4(n-1)+2, RBL4(n-1)+3, and RBL4(n-1)+4 are arranged in correspondence with the four MTJ elements 12 in one read block BKik.

[0547] The read bit lines RBL4(n-1)+1, RBL4(n-1)+2, RBL4(n-1)+3, and RBL4(n-1)+4 run in the X-direction. One end of each read bit line is connected to a common data line 30A through the row select switch (MOS transistor) RSW2. The common data line 30A is connected to a read circuit 29B (including, e.g., a sense amplifier, selector, and output buffer).

[0548] For example, as shown in FIGS. 120 and 130, the read bit line is connected to a bias transistor BT which sets the bit line potential to VC.

[0549] A row select line signal RLi (i = 1,..., n) is input to each row select switch RSW2. Row decoders 25-1,..., 25-n output the row select line signals RLi.

[0550] As shown in FIG. 120, the bias transistor BT is a PMOS transistor, when the RLi is input to the bias transistor BT. As shown in FIG. 130, the bias transistor BT is a NMOS transistor, when the inverting signal from RLi is input to the bias transistor BT. Row decoders 25-1,..., 25-n output the row select line signals RLi and the inverting signal thereof.

[0551] In this example, the read bit lines RBL4(n-1)

+1, RBL4(n-1)+2, RBL4(n-1)+3, and RBL4(n-1)+4 run in the X-direction and also function as write bit lines WBL4(n-1)+1, WBL4(n-1)+2, WBL4(n-1)+3, and WBL4 (n-1)+4, respectively.

[0552] One end of each of the write bit lines WBL4(n-1)+1, WBL4(n-1)+2, WBL4(n-1)+3, and WBL4(n-1)+4 is connected to a write bit line driver/sinker 23AR through the row select switches RSW2 and common data line 30A. The other end of each write bit line is connected to a write bit line driver/sinker 23AS through a common data line 30B.

[0553] One write word line WWLi (i = 1,..., j) which is shared by the four MTJ elements 12 of one read block BKik and run in the Y-direction is arranged near the MTJ elements 12 constituting the read block BKik. One write word line WWLi is arranged in one column.

[0554] One end of each write word line WWLi is connected to a circuit block 29AR including a column decoder and write word line driver. The other end is connected to a circuit block 31R including a column decoder and write word line sinker.

[0555] In write operation, the circuit blocks 29AR and 31R are set in an operative state. A write current flows to the write word lines WWLi in a direction from the circuit block 29AR to the circuit 31R.

[0556] In the write operation, the row decoder 25-n selects one of the plurality of rows on the basis of a row address signal. The write bit line drivers/sinkers 23AR and 23AS supply a write current having a direction corresponding to write data to one of the write bit lines WBL4(n-1)+1, WBL4(n-1)+2, WBL4(n-1)+3, and WBL4 (n-1)+4 in the selected row.

[0557] In the read operation, the row decoder 25-n selects one of the plurality of rows on the basis of a row address signal.

[0558] A column decoder 32 selects one of the plurality of columns on the basis of column address signals and outputs column select signals CSL1,..., CSLj. The column select switch CS Warranted in the selected column is turned on.

② Device Structure

[0559] The device structure will be described next.

[1] Sectional Structure

[0560] FIG. 54 shows a device structure corresponding to one block of the magnetic random access memory according to Structural Example 7 of the present invention.

[0561] The same reference numerals as in FIG. 53 denote the same elements in FIG. 54 to show the correspondence between the elements.

[0562] A read word line RWL1 running in the Y-direction is formed on a semiconductor substrate 41. No switch element is arranged immediately under the read word line RWL1. Four MTJ elements (Magnetic Tunnel Junction elements) MTJ1, MTJ2, MTJ3, and MTJ4 arrayed in the Y-direction are formed above the read word line RWL1.

[0563] One terminal (upper end in this example) of each of the MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4 is commonly connected to an upper electrode 44. A contact plug 42 and conductive layer 43 electrically connects the upper electrode 44 to the read word line RWL1.

[0564] The contact portion between the upper electrode 44 and the read word line RWL1 is formed in the region between the MTJ elements MTJ1 and MTJ2 and the MTJ elements MTJ3 and MTJ4. When the MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4 are uniformly arranged to be symmetrical with respect to the contact portion, signal margin in the read operation due to the interconnection resistance or the like can be maximized.

[0565] The conductive layer 43 may be integrated with the upper electrode 44. That is, the conductive layer 43 and upper electrode 44 may be formed simultaneously using the same material.

[0566] The other terminal (lower end in this example) of each of the MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4 is electrically connected to a corresponding one of the read bit lines RBL1, RBL2, RBL3, and RBL4 (write bit lines WBL1, WBL2, WBL3, and WBL4). The read bit lines RBL1, RBL2, RBL3, and RBL4 run in the X-direction (row direction).

[0567] The MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4 are independently connected to the read bit lines RBL1, RBL2, RBL3, and RBL4, respectively. That is, the four read bit lines RBL1, RBL2, RBL3, and RBL4 are arranged in correspondence with the four MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4.

[0568] The write word line WWL1 is formed immediately on and near the MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4. The write word line WWL1 runs in the Y-direction (column direction).

[0569] In this example, one write word line WWL1 is arranged in correspondence with the four MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4 which construct a read block. Instead, for example, the four MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4 may be stacked, and four write word lines may be arranged in correspondence with the four MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4.

[0570] In this example, the write word line WWL1 running in the Y-direction is arranged above the MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4, and the read bit lines RBL1, RBL2, RBL3, and RBL4 running in the X-direction are arranged under the MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4.

[0571] Instead, for example, the write word line WWL1 running in the Y-direction may be arranged under the MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4, and the read bit lines RBL1, RBL2, RBL3, and RBL4 running in the X-direction are arranged above the MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4.

[0572] According to this device structure, the plurality of MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4 in the read block are electrically connected to the different read bit lines RBL1, RBL2, RBL3, and RBL4 (write bit lines WBL1, WBL2, WBL3, and WBL4), respectively. For this reason, data of the plurality of MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4 in the read block can be read at once by one read step.

[0573] One terminal of each of the plurality of MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4 in the read block is commonly connected. The connection point is directly connected to the read word line RWL1 without intervening a read select switch. In addition, the write word line WWL1 running in the Y-direction is shared by the plurality of MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4 in the read block. For this reason, the degree of integration of MTJ elements can be increased, and their characteristic can be improved.

[Plane Structure]

[0574] FIGS. 55 to 57 show the layouts of the respective interconnection layers in device structure shown in FIG. 54. The section shown in FIG. 54 corresponds to the section taken along a line LIV - LIV in FIGS. 55 to 57.

[0575] FIG. 5 shows the layout of read word lines.

[0576] The read word lines RWL1 run in the Y-direction. The contact plug 42 is arranged on each read word line RWL1.

[0577] FIG. 56 shows the layout of the read bit lines and MTJ elements.

[0578] The read bit lines RBL1, RBL2, RBL3, and RBL4 (write bit lines WBL1, WBL2, WBL3, and WBL4) run in the X-direction. The interval between the read bit lines RBL1, RBL2, RBL3, and RBL4 can be set to, e.g., the minimum size (or design rule) processible by photolithography.

[0579] The MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4 are arranged on the read bit lines RBL1, RBL2, RBL3, and RBL4, respectively. The axis of easy magnetization of the MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4, i.e., the direction parallel to the long sides of the MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4 is the Y-direction.

[0580] The read bit line RBL1 is commonly connected to the MTJ elements MTJ1 arranged in the X-direction. The read bit line RBL2 is commonly connected to the MTJ elements MTJ2 arranged in the X-direction. The read bit line RBL3 is commonly connected to the MTJ elements MTJ3 arranged in the X-direction. The read bit line RBL4 is commonly connected to the MTJ elements MTJ4 arranged in the X-direction.

[0581] The conductive layer 43 is arranged on the contact plug 42.

[0582] FIG. 57 shows the layout of write bit lines.

[0583] The upper electrode 44 having a rectangular pattern is arranged on the MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4 and conductive layer 43. The upper electrode 44 are in contact with the MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4 and conductive layer 43.

[0584] The write word lines WWL1 are arranged immediately on the upper electrodes 44. The write word lines WWL1 run in the Y-direction.

(8) Structural Examples 8, 9, and 10

[0585] Structural Examples 8, 9, and 10 as improvements of Structural Example 1 will now be described.

① Structural Example 8

[0586] FIG. 58 shows the main part of a magnetic random access memory according to Structural Example 8 of the present invention.

[0587] As a characteristic feature of Structural Example 8, in read operation, a bias voltage VC is applied to one terminal of each of four MTJ elements 12 that form a read block BKik.

[0588] More specifically, in Structural Example 1 (FIG. 1), the read word line RWLi is connected to the ground point VSS through the column select switch CSW, and the bias voltage VC is generated by the read circuit 29B. In Structural Example 8, a read word line RWLi is connected to a bias line 34 through a column select switch CSW, and the bias voltage VC is supplied to the bias line 34.

[0589] Hence, in the read operation, the bias voltage VC can be applied to the bias line 34, and a read current can be supplied from the bias line 34 to the MTJ element 12. In a mode (e.g., write operation) except the read operation, a ground potential VSS is applied to the bias line 34.

[0590] In Structural Example 8, the potential of the read word line RWLi can be changed. Hence, in the read operation, the bias voltage VC can be applied to the read word line RWLi, and the read current can be supplied to the MTJ element 12 in the read block BKik.

[0591] For example, as shown in FIG. 131, the read bit line is connected to a bias transistor BT which sets the bit line potential to VC.

[0592] A row select line signal RLi (i = 1,..., n) is input to each row select switch RSW2. Row decoders 25-1,..., 25-n output the row select line signals RLi.

[0593] As shown in FIG. 131, the bias transistor BT is a NMOS transistor, when the inverting signal from RLi is input to the bias transistor BT. Row decoders 25-1,..., 25-n output the row select line signals RLi and the inverting signal thereof.

② Structural Example 9

[0594] FIG. 59 shows the main of a magnetic random access memory according to Structural Example 9 of the present invention.

[0595] As a characteristic feature of Structural Example 9, a write word line driver is arranged in one row of

a memory cell array.

[0596] In Structural Example 1 (FIG. 1), only one write word line driver 23A is commonly arranged for all rows of the memory cell array 11 and connected to the common data line (common driver line) 30. In this case, however, elements having resistances, i.e., the common data line and row select switches are connected between the write word line driver and the write word line. Since a voltage drop due to these elements becomes large, the write current becomes small.

[0597] In Structural Example 9, write word line drivers 33-1,..., 33-n are arranged for rows of a memory cell array 11, respectively.

[0598] More specifically, in each row of the memory cell array 11, a corresponding one of the write word line drivers 33-1,..., 33-n is connected between row select switches RSW2 and write word lines WWL4(n-1)+1, WWL4(n-1)+2, WWL4(n-1)+3, and WWL4(n-1)+4.

[0599] In this case, the write word line drivers 33-1,..., 33-n need to drive only the write word lines WWL4(n-1)+1, WWL4(n-1)+2, WWL4(n-1)+3, and WWL4(n-1)+4.

[0600] Hence, the driving force for the write word line drivers 33-1,..., 33-n can be decreased. This contributes to decreasing power consumption and increasing the operation speed.

[0601] Since the read current is much smaller than the write current, the driving force of the row select switches RSW2 need not be increased.

[0602] The write word line drivers 33-1,..., 33-n are controlled by output signals (word line enable signals) WLEN1,..., WLEN4 from row decoders 25-1,..., 25-n. More specifically, in the write operation, the row decoders 25-1,..., 25-n are activated to select one row. In the selected row, one of the output signals (word line enable signals) WLEN1,..., WLEN4 changes to "H".

[0603] In Structural Example 1, the row select switches RSW2 are controlled by the output signals from the row decoders 25-1,..., 25-n which are activated only in the write operation. In Structural Example 9, the row select switches RSW2 are controlled by the output signals from circuit blocks 23B-1,..., 23B-n each including a row decoder and read line driver.

[0604] That is, the gates of the row select switches (MOS transistors) RSW2 are connected to read lines RW1,..., RWn.

[0605] The reason why this structure is employed is as follows. The write word line drivers 33-1,..., 33-n are arranged for the respective rows. Hence, in the write operation, all the write word lines WWL4(n-1)+1, WWL4(n-1)+2, WWL4(n-1)+3, and WWL4(n-1)+4 must be disconnected from the common data line 30.

[0606] More specifically, the circuit blocks 23B-1,..., 23B-n each including a row decoder and read line driver are activated only in the read operation. In the write operation, the row select switches RSW2 of all rows are turned off, so all the write word lines WWL4(n-1)+1, WWL4(n-1)+2, WWL4(n-1)+3, and WWL4(n-1)+4 are disconnected from the common data line 30.

[0607] For example, as shown in FIG. 132, the read bit line is connected to a bias transistor BT which sets the bit line potential to VC.

[0608] A row select line signal RWi (i = 1,..., n) is input to each row select switch RSW2. Row decoders 23B-1,..., 23B-n output the row select line signals RWi.

[0609] As shown in FIG. 132, the bias transistor BT is a NMOS transistor, when the inverting signal from RLi is input to the bias transistor BT. Row decoders 23B-1,..., 23B-n output the row select line signals RWi and the inverting signal thereof.

③ Structural Example 10

[0610] FIG. 60 shows the main part of a magnetic random access memory according to Structural Example 10 of the present invention.

[0611] As a characteristic feature of Structural Example 10, MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4 in a plurality of or all read blocks BKIx and BK1(x+1) in one column (Y-direction) share one upper electrode 44.

[0612] In Structural Example 1, the upper electrode 44 for the MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4 is arranged for each read block. However, the upper electrodes 44 for the MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4 in read blocks in one column are short-circuited through the read word line RWL1.

[0613] Hence, the upper electrodes 44 for the MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4 in the read blocks in one column may be short-circuited. However, the upper electrodes 44 for the MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4 in read blocks in one row (X-direction) must be disconnected from each other.

[0614] In Structural Example 10, the MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4 in the plurality of or all the read blocks BKIx and BK1(x+1) in one column share one upper electrode 44.

[0615] According to Structural Example 10, since no contact plug 42 must be arranged for each read block, the density of MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4 can be increased. That is, theoretically, at least one contact plug 42 suffices between a read word line RWL1 and the shared upper electrode 44. Actually, a plurality of contact plugs 42 are preferably arranged in one column equidistantly in consideration of the interconnection resistance and the like.

[0616] Structural Example 10 has been described as a modification of Structural Example 1. However, Structural Example 10 can be applied to all of Structural Examples 2 to 9.

(9) Others

[0617] As described above, the present invention is applied to a magnetic random access memory which has a cell array structure in which one terminal of each of a plurality of MTJ elements of a read block is commonly connected, and the other terminal is independ-

ently connected to a read bit line. When a select switch (e.g., a MOS transistor) is arranged in a read block, the degree of integration of MTJ elements can hardly be increased.

[0618] Normally, a select switch is formed in the surface region of a semiconductor substrate. An MTJ element is formed above the select switch. In this case, a contact hole is necessary for electrically connecting the select switch and MTJ element. That is, since no MTJ element can be arranged in the region where the contact hole is formed, the area of the memory cell array increases.

[0619] On the other hand, the resistance value of the MTJ element which forms a memory cell of the magnetic random access memory is sufficiently large. The read current is much smaller than the write current. That is, even when the select transistor in the read block is omitted, an increase in current consumption due to the read current flowing to MTJ elements in an unselected block poses no serious problem.

[0620] In the present invention, first, in the cell array structure in which one terminal of each of the plurality of MTJ elements of a read block is independently connected to a read bit line, the select switch which selects a read block is omitted. That is, no select switch (MOS transistor) is arranged in the memory cell array (immediately under the MTJ elements).

[0621] According to the characteristic feature of the present invention, since no select switch is present in the memory cell array, the MTJ elements can be arranged at a high density. In addition, since no select switch (semiconductor element) is present immediately under the MTJ elements, the planarity of the underlying layer of the MTJ elements can be improved, and the characteristics (uniform MR ratio or the like) of the MTJ elements can be improved.

[0622] To further improve the planarity of the underlying layer of the MTJ elements, a dummy pattern, e.g., a dummy interconnection pattern which does not function as an actual interconnection is arranged immediately under the MTJ elements.

[0623] Normally, to reduce the manufacturing cost (proportional to the number of times of PEP, the members (MTJ elements and the like) of the memory cell array portion and the members (interconnections) of the peripheral circuit portion are simultaneously processed as much as possible. However, when no select switch is present immediately under the MTJ elements, a step difference is generated between the memory cell array portion and the peripheral circuit portion. This step difference degrades the process accuracy of photolithography.

[0624] To prevent this, a dummy pattern is arranged immediately under the MTJ elements to increase the planarity of the underlying layer of the MTJ elements. More specifically, the step difference between the memory cell array portion and the peripheral circuit portion is eliminated. As the dummy pattern, a periodical (a repeat of a predetermined pattern) or a pattern which is uniform as a whole is used.

[0625] When the plurality of MTJ elements in a read block are arrayed in a direction parallel to the surface of the semiconductor substrate, i.e., arrayed in a line in the horizontal direction, a plurality of stages of memory cell arrays are stacked. When no select switch is present in the read block, a plurality of stages of memory cell arrays can be stacked.

[0626] The MTJ elements are also arranged in a direction perpendicular to the surface of the semiconductor substrate, i.e., in the vertical direction. That is, since the MTJ elements are arranged three-dimensionally, the density of MTJ elements can be increased as compared to a two-dimensional cell array structure. In addition, when a predetermined interconnection is shared by the memory cell array of the upper stage and that of the lower stage, the manufacturing cost can be reduced, and the insulating layer of each stage can be planarized (the characteristic of the MTJ elements can be increased).

[0627] In the cell array structure having the above characteristic features, an interconnection which functions only as a read bit line is connected to one terminal of each of the plurality of MTJ elements of a read block. That is, one of two write lines for a write is not electrically connected to the plurality of MTJ elements.

[0628] Hence, in the write operation, even when a potential difference is generated due to the interconnection resistance of the two write lines, the potential difference is not generated across the MTJ elements. According to the device structure of the present invention, dielectric breakdown (breakdown of the tunneling barrier layer of the MTJ element) in the write operation poses no problem, unlike a cross-point cell array structure.

[0629] As a switch for the magnetic random access memory, a MIS (Metal Insulator Semiconductor) transistor (including a MOS transistor), MES (Metal Semiconductor) transistor, junction transistor, bipolar transistor, or diode can be used.

2. Structural Examples of MTJ Element

[0630] FIGS. 61 to 63 show structural examples of the MTJ element.

[0631] The MTJ element shown in FIG. 61 has the most basic structure having two ferromagnetic layers and a tunneling barrier layer sandwiched between these layers.

[0632] An antiferromagnetic layer for fixing the magnetizing direction is added to a fixed layer (pinning layer) of the two ferromagnetic layers, in which the magnetizing direction is fixed. The magnetizing direction in a free layer (storing layer) of the two ferromagnetic layers, in which the magnetizing direction can be freely changed, is determined by a synthesized magnetic field formed by a write word line and write bit line.

[0633] The MTJ element shown in FIG. 62 has two tunneling barrier layers in it to make the bias voltage

higher than in the MTJ element shown in FIG. 61.

[0634] The MTJ element shown in FIG. 62 can be regarded to have a structure (double junction structure) in which two MTJ elements shown in FIG. 61 are connected in series.

[0635] In this example, the MTJ element has three ferromagnetic layers. Tunneling barrier layers are inserted between the ferromagnetic layers. Antiferromagnetic layers are added to the two ferromagnetic layers (pinning layers) at two ends. The middle layer in the three ferromagnetic layers serves as a free layer (storing layer) in which the magnetizing direction can be freely changed.

[0636] The MTJ element shown in FIG. 63 can easily close lines of magnetic force in the ferromagnetic layer serving as a storing layer, as compared to the MTJ element shown in FIG. 61.

[0637] For the MTJ element of this example, it can be regarded that the storing layer of the MTJ element shown in FIG. 61 is replaced with a storing layer formed from two ferromagnetic layers and a nonmagnetic metal layer (e.g., an aluminum layer) sandwiched between those layers.

[0638] When the storing layer of the MTJ element has a three-layered structure made of two ferromagnetic layers and a nonmagnetic metal layer sandwiched between these layers, lines of magnetic force in the two ferromagnetic layers of the storing layer readily close. That is, since any antimagnetic field component in the two ferromagnetic layers of the storing layer can be prevented, the MR ratio can be improved.

[0639] The structural examples of the MTJ element have been described above. In the present invention (circuit structure, device structure, read operation principle, read circuit, and manufacturing method), the structure of the MTJ element is not particularly limited. The above-described three structural examples are mere representative examples of the MTJ element structure.

3. Examples of Peripheral Circuits

[0640] Circuit examples of the write word line driver/sinker, circuit examples of the write bit line driver/sinker, circuit examples of the read word line driver, circuit examples of the row decoder, circuit examples of the column decoder, and circuit examples of a read circuit (including a sense amplifier) will be sequentially described below.

(1) Write Word Line Driver/Sinker

[0641] FIG. 64 shows a circuit example of the write word line driver/sinker.

[0642] Assume that a read block is formed from four MTJ elements, and each of the four MTJ elements is selected by lower two bits CA0 and CA1 of a column address signal. FIG. 64 shows a write word line driver/sinker of only one row.

[0643] The write word line driver 23A includes PMOS transistors QP1, QP2, QP3, and QP4, and NAND gate circuits ND1, ND2, ND3, and ND4. The write word line sinker 24-n is formed from NMOS transistors QN1, QN2, QN3, and QN4.

[0644] The source of the PMOS transistor QP1 is connected to a power supply terminal VDD. The drain is connected to one end of the write word line WWL4(n-1)+1 through the common data line (common driver line) 30 and row select switch RSW2. The output terminal of the NAND gate circuit ND1 is connected to the gate of the PMOS transistor QP1. The source of the NMOS transistor QN1 is connected to the ground terminal VSS. The drain is connected to the other end of the write word line WWL4(n-1)+1.

[0645] When the output signal from the NAND gate circuit ND1 is "0", a write current flows to the write word line WWL4(n-1)+1 in the selected row (the row whose row select switch RSW2 is turned on).

[0646] The source of the PMOS transistor QP2 is connected to the power supply terminal VDD. The drain is connected to one end of the write word line WWL4(n-1)+2 through the common data line (common driver line) 30 and row select switch RSW2. The output terminal of the NAND gate circuit ND2 is connected to the gate of the PMOS transistor QP2. The source of the NMOS transistor QN2 is connected to the ground terminal VSS. The drain is connected to the other end of the write word line WWL4(n-1)+2.

[0647] When the output signal from the NAND gate circuit ND2 is "0", a write current flows to the write word line WWL4(n-1)+2 in the selected row (the row whose row select switch RSW2 is turned on).

[0648] The source of the PMOS transistor QP3 is connected to the power supply terminal VDD. The drain is connected to one end of the write word line WWL4(n-1)+3 through the common data line (common driver line) 30 and row select switch RSW2. The output terminal of the NAND gate circuit ND3 is connected to the gate of the PMOS transistor QP3. The source of the NMOS transistor QN3 is connected to the ground terminal VSS. The drain is connected to the other end of the write word line WWL4(n-1)+3.

[0649] When the output signal from the NAND gate circuit ND3 is "0", a write current flows to the write word line WWL4(n-1)+3 in the selected row (the row whose row select switch RSW2 is turned on).

[0650] The source of the PMOS transistor QP4 is connected to the power supply terminal VDD. The drain is connected to one end of the write word line WWL4(n-1)+4 through the common data line (common driver line) 30 and row select switch RSW2. The output terminal of the NAND gate circuit ND4 is connected to the gate of the PMOS transistor QP4. The source of the NMOS transistor QN4 is connected to the ground terminal VSS. The drain is connected to the other end of the write word line WWL4(n-1)+4.

[0651] When the output signal from the NAND gate circuit ND4 is "0", a write current flows to the write word line WWL4(n-1)+4 in the selected row (the row whose row select switch RSW2 is turned on).

[0652] A write signal WRITE is input to the NAND gate circuits ND1, ND2, ND3, and ND4. In the write operation, the write signal WRITE changes to "H". In addition, different lower column address signals CA0, /CA0, CA1, and /CA1 are input to the NAND gate circuits ND1, ND2, ND3, and ND4.

[0653] That is, in this example, column address signal bits bCA0 and bCA1 are used to select one write word line WWL4(n-1)+1 of the four write word lines (read bit lines) in the selected row and input to the NAND circuit ND1.

[0654] Column address signal bits CA0 and bCA1 are used to select one write word line WWL4(n-1)+2 of the four write word lines (read bit lines) in the selected row and input to the NAND circuit ND2.

[0655] Column address signal bits bCA0 and CA1 are used to select one write word line WWL4(n-1)+3 of the four write word lines (read bit lines) in the selected row and input to the NAND circuit ND3.

[0656] The column address signal bits CA0 and CA1 are used to select one write word line WWL4(n-1)+4 of the four write word lines (read bit lines) in the selected row and input to the NAND circuit ND4.

[0657] Note that the signal bits bCA0 and bCA1 are inverted signal bits with inverted levels of CA0 and CA1.

[0658] In this write word line driver/sinker, in the write operation, the write signal WRITE changes to "H". For example, one of the output signals from the four NAND gate circuits ND1, ND2, ND3, and ND4 changes to "L".

[0659] For example, when both CA0 and CA1 are "0", all input signals to the NAND gate circuit ND1 are "1". The output signal from the NAND gate circuit ND1 is "0". As a result, the PMOS transistor QP1 is turned on. The write current flows to the write word line WWL4(n-1)+1.

[0660] When CA0 is "1" and CA1 is "0", all input signals to the NAND gate circuit ND2 are "1". The output signal from the NAND gate circuit ND2 is "0". As a result, the PMOS transistor QP2 is turned on. The write current flows to the write word line WWL4(n-1)+2.

[0661] When CA0 is "0" and CA1 is "1", all input signals to the NAND gate circuit ND3 are "1". The output signal from the NAND gate circuit ND3 is "0". As a result, the PMOS transistor QP3 is turned on. The write current flows to the write word line WWL4(n-1)+3.

[0662] When both CA0 and CA1 are "1", all input signals to the NAND gate circuit ND4 are "1". The output signal from the NAND gate circuit ND4 is "0". As a result, the PMOS transistor QP4 is turned on. The write current flows to the write word line WWL4(n-1)+4.

(2) Write Bit Line Driver/Sinker

[0663] FIG. 65 shows a circuit example of the write bit line driver/sinker.

[0664] The write bit line driver/sinker 29A is formed from PMOS transistors QP5 and QP6, NMOS transistors QN5 and QN6, NAND gate circuits ND5 and ND6, AND gate circuits AD1 and AD2, and inverters INV1 and INV2.

[0665] The PMOS transistor QP5 is connected between the power supply terminal VDD and one end of the write bit line WBL1. The output signal from the NAND gate circuit ND5 is supplied to the gate of the PMOS transistor QP5. The NMOS transistor QN5 is connected between one end of the write bit line WBL1 and the ground terminal VSS. The output signal from the AND gate circuit AD1 is supplied to the gate of the NMOS transistor QN5.

[0666] The PMOS transistor QP6 is connected between the power supply terminal VDD and one end of the write bit line WBLj. The output signal from the NAND gate circuit ND6 is supplied to the gate of the PMOS transistor QP6. The NMOS transistor QN6 is connected between one end of the write bit line WBLj and the ground terminal VSS. The output signal from the AND gate circuit AD2 is supplied to the gate of the NMOS transistor QN6.

[0667] The write bit line driver/sinker 31 is formed from PMOS transistors QP7 and QP8, NMOS transistors QN7 and QN8, NAND gate circuits ND7 and ND8, AND gate circuits AD3 and AD4, and inverters INV3 and INV4.

[0668] The PMOS transistor QP7 is connected between the power supply terminal VDD and the other end of the write bit line WBL1. The output signal from the NAND gate circuit ND7 is supplied to the gate of the PMOS transistor QP7. The NMOS transistor QN7 is connected between the other end of the write bit line WBL1 and the ground terminal VSS. The output signal from the AND gate circuit AD3 is supplied to the gate of the NMOS transistor QN7.

[0669] The PMOS transistor QP8 is connected between the power supply terminal VDD and the other end of the write bit line WBLj. The output signal from the NAND gate circuit ND8 is supplied to the gate of the PMOS transistor QP8. The NMOS transistor QN8 is connected between the other end of the write bit line WBLj and the ground terminal VSS. The output signal from the AND gate circuit AD4 is supplied to the gate of the NMOS transistor QN8.

[0670] In the write bit line drivers/sinkers 29A and 31 with the above structures, when the output signal from the NAND gate circuit ND5 is "0", and the output signal from the AND gate circuit AD3 is "1", a write current from the write bit line driver/sinker 29A to the write bit line driver/sinker 31 flows to the write bit line WBL1.

[0671] When the output signal from the NAND gate circuit ND7 is "0", and the output signal from the AND gate circuit AD1 is "1", a write current from the write bit line driver/sinker 31 to the write bit line driver/sinker 29A flows to the write bit line WBL1.

[0672] In the write bit line drivers/sinkers 29A and 31,

in the write operation, the write signal WRITE is "1". In the selected column, all bits of the upper column address signal are "1". Hence, a write current having a direction corresponding to the value of write data DATA flows to the write bit line WBLi (i = 1,..., j) in the selected column.

[0673] The direction of write current flowing to the write bit line WBLi in the selected column is determined in accordance with the value of the write data DATA.

[0674] For example, when the write bit line WBL1 is selected, and the write data DATA is "1", the output signal from the NAND gate circuit ND5 is "0". The output signal from the AND gate circuit AD3 is "1". As a result, a write current from the write bit line driver/sinker 29A to the write bit line driver/sinker 31 flows to the write bit line WBL1.

[0675] Conversely, when the write data DATA is "0", the output signal from the NAND gate circuit ND7 is "0". The output signal from the AND gate circuit AD1 is "1". As a result, a write current from the write bit line driver/sinker 31 to the write bit line driver/sinker 29A flows to the write bit line WBL1.

(3) Row Decoder

[0676] FIG. 66 shows a circuit example of the row decoder.

[0677] The row decoder 25-1 can have, e.g., the following structure. FIG. 66 shows the row decoder of only one row.

[0678] The row decoder 25-1 is formed from an AND gate circuit AD11. A row address signal is input to the AND gate circuit AD11. In the selected row, all the bits of the row address signals are "H". Hence, an output signal RL1 from the row decoder 25-1 changes to "H".

(4) Column Decoder & Read Column Select Line Driver

[0679] FIG. 67 shows a circuit example of the column decoder & read column select line driver.

[0680] FIG. 67 illustrates the column decoder & read column select line driver of only one column of the memory cell array.

[0681] The column decoder & read column select line driver 32 is formed from an AND gate circuit AD10. A read signal READ and upper column address signal are input to the AND gate circuit AD10.

[0682] In the read operation, the read signal changes to "H". That is, in a mode other than the read operation, the potential of the output signal (column select signal) CSL1 from the column decoder & read column select line driver 32 does not change to "H". In the read operation, in the selected column, all bits of the column address signal are "H". Hence, the potential of the output signal CSL1 from the column decoder & read column select line driver 32 changes to "H".

(5) Write Bit Line Driver/Sinker

[0683] A circuit example of the write bit line driver/sinker used in Structural Example 7 (FIG. 53) will be described.

[0684] FIGS. 68 and 69 show a circuit example of the write bit line driver/sinker.

[0685] The write bit line driver/sinker 23AR is formed from PMOS transistors QP5, QP6, QP7, and QP8, NMOS transistors QN5, QN6, QN7, and QN8, NAND gate circuits ND5, ND6, ND7, and ND8, AND gate circuits AD1, AD2, AD3, and AD4, and inverters INV1, INV2, INV3, and INV4.

[0686] The PMOS transistor QP5 is connected between the power supply terminal VDD and the common data line 30A. The output signal from the NAND gate circuit ND5 is supplied to the gate of the PMOS transistor QP5. The NMOS transistor QN5 is connected between the common data line 30A and the ground terminal VSS. The output signal from the AND gate circuit AD1 is supplied to the gate of the NMOS transistor QN5.

[0687] The PMOS transistor QP6 is connected between the power supply terminal VDD and the common data line 30A. The output signal from the NAND gate circuit ND6 is supplied to the gate of the PMOS transistor QP6. The NMOS transistor QN6 is connected between the common data line 30A and the ground terminal VSS. The output signal from the AND gate circuit AD2 is supplied to the gate of the NMOS transistor QN6.

[0688] The PMOS transistor QP7 is connected between the power supply terminal VDD and the common data line 30A. The output signal from the NAND gate circuit ND7 is supplied to the gate of the PMOS transistor QP7. The NMOS transistor QN7 is connected between the common data line 30A and the ground terminal VSS. The output signal from the AND gate circuit AD3 is supplied to the gate of the NMOS transistor QN7.

[0689] The PMOS transistor QP8 is connected between the power supply terminal VDD and the common data line 30A. The output signal from the NAND gate circuit ND8 is supplied to the gate of the PMOS transistor QP8. The NMOS transistor QN8 is connected between the common data line 30A and the ground terminal VSS. The output signal from the AND gate circuit AD4 is supplied to the gate of the NMOS transistor QN8.

[0690] The write bit line driver/sinker 23AS is formed from PMOS transistors QP9, QP10, QP11, and QP12, NMOS transistors QN9, QN10, QN11, and QN12, NAND gate circuits ND9, ND10, ND11, and ND12, AND gate circuits AD5, AD6, AD7, and AD8, and inverters INV5, INV6, INV7, and INV8.

[0691] The PMOS transistor QP9 is connected between the power supply terminal VDD and the common data line 30B. The output signal from the NAND gate circuit ND9 is supplied to the gate of the PMOS transistor QP9. The NMOS transistor QN9 is connected between the common data line 30B and the ground terminal VSS. The output signal from the AND gate circuit

AD5 is supplied to the gate of the NMOS transistor QN9.

[0692] The PMOS transistor QP10 is connected between the power supply terminal VDD and the common data line 30B. The output signal from the NAND gate circuit ND10 is supplied to the gate of the PMOS transistor QP10. The NMOS transistor QN10 is connected between the common data line 30B and the ground terminal VSS. The output signal from the AND gate circuit AD6 is supplied to the gate of the NMOS transistor QN10.

[0693] The PMOS transistor QP11 is connected between the power supply terminal VDD and the common data line 30B. The output signal from the NAND gate circuit ND11 is supplied to the gate of the PMOS transistor QP11. The NMOS transistor QN11 is connected between the common data line 30B and the ground terminal VSS. The output signal from the AND gate circuit AD7 is supplied to the gate of the NMOS transistor QN11.

[0694] The PMOS transistor QP12 is connected between the power supply terminal VDD and the common data line 30B. The output signal from the NAND gate circuit ND12 is supplied to the gate of the PMOS transistor QP12. The NMOS transistor QN12 is connected between the common data line 30B and the ground terminal VSS. The output signal from the AND gate circuit AD8 is supplied to the gate of the NMOS transistor QN12.

[0695] In the write bit line drivers/sinkers 23AR and 23AS with the above structures, for example, when the output signal from the NAND gate circuit ND5 is "0", and the output signal from the AND gate circuit AD5 is "1", a write current from the write bit line driver/sinker 23AR to the write bit line driver/sinker 23AS flows to the write bit line WBL4(n-1)+1 in the row selected by the row select switch RSW2.

[0696] For example, when the output signal from the NAND gate circuit ND9 is "0", and the output signal from the AND gate circuit AD1 is "1", a write current from the write bit line driver/sinker 2AS to the write bit line driver/sinker 23AR flows to the write bit line WBL4(n-1)+1 in the row selected by the row select switch RSW2.

[0697] In the write bit line drivers/sinkers 23AR and 23AS, in the write operation, the write signal WRITE is "1". In this example, one read block BKik is selected by the row address signal and upper column address signal (signal bits except lower two bits of the column address signal).

[0698] The four MTJ elements are present in the selected read block BKik. To select one of the four MTJ elements, the lower two bits CAD and CA1 of the column address signal are used.

[0699] The direction of write current flowing to the write bit line WBL4(n-1)+1, which is to be used to write data in the selected MTJ element in the selected read block BKik, is determined in accordance with the value of the write data DATA.

[0700] For example, when the write bit line WBL4(n-1)+1 is selected, and the write data DATA is "1", the output signal from the NAND gate circuit ND5 is "0". The output signal from the AND gate circuit AD5 is "1". As a result, a write current from the write bit line driver/sinker 23AR to the write bit line driver/sinker 23AS flows to the write bit line WBL4(n-1)+1.

[0701] Conversely, when the write data DATA is "0", the output signal from the NAND gate circuit ND9 is "0". The output signal from the AND gate circuit AD1 is "1". As a result, a write current from the write bit line driver/sinker 23AS to the write bit line driver/sinker 23AR flows to the write bit line WBL4(n-1)+1.

(6) Column Decoder & Write Word Line Driver/Sinker

[0702] A circuit example of the column decoder & write word line driver/sinker used in Structural Example 7 (FIG. 53) will be described.

[0703] FIG. 70 shows a circuit example of a column decoder & write word line driver/sinker.

[0704] The column decoder & write word line driver/sinker 29AR is formed from NAND gate circuits ND1,..., NDj and PMOS transistor QP1,..., QPj.

[0705] Each of the PMOS transistor QP1,..., QPj is connected between the power supply terminal VDD and one end of a corresponding one of write word lines WWL1,..., WWLj. The output signals from the NAND gate circuits ND1,..., NDj are supplied to the gates of the PMOS transistor QP1,..., QPj, respectively.

[0706] In the write operation, the write signal WRITE is "1". In the selected column, all the upper column address signal bits are "1". Hence, the output signals from the NAND gate circuits ND1,..., NDj are "0", and the PMOS transistor QP1,..., QPj are turned on.

[0707] The write word line sinker 31R is formed from NMOS transistor QN1,..., QNj.

[0708] Each of the NMOS transistor QN1,..., QNj is connected between the ground terminal VSS and the other end of a corresponding one of the write word lines WWL1,..., WWLj. The NMOS transistor QN1,..., QNj are always ON because the power supply potential VDD is supplied to their gates.

(7) Row Decoder

[0709] A circuit example of the row decoder used in Structural Example 9 (FIG. 59) will be described.

[0710] FIG. 71 shows a circuit example of the row decoder.

[0711] FIG. 71 shows the row decoder 25-1 of only one row.

[0712] The row decoder 25-1 is formed from four AND gate circuit AD13 to AD16. The write signal WRITE, row address signal, and lower two bits CA0 and CA1 of the column address signal are input to the AND gate circuit AD13 to AD16.

[0713] In the write operation, the write signal WRITE changes to "H". In the selected row, all bits of the row

address signal change to "H". In the selected row, one of the four MTJ elements in the selected read block, i. e., one of the four write word lines is selected on the basis of the lower two bits CA0 and CA1 of the column address signal.

(8) Write Word Line Driver

[0714] A circuit example of the write word line driver used in Structural Example 9 (FIG. 59) will be described.

[0715] FIG. 72 shows a circuit example of the write word line driver.

[0716] FIG. 72 shows the write word line driver of only one row.

[0717] The write word line driver 33-1 is formed from PMOS transistors P1, P2, P3, and P4 connected to the write word lines WWL1, WWL2, WWL3, and WWL4, respectively.

[0718] Each of the PMOS transistors P1, P2, P3, and P4 is connected between the power supply terminal VDD and a corresponding one of the write word lines WWL1, WWL2, WWL3, and WWL4 and controlled by a corresponding one of word line enable signals WLEN1 to WLEN4. The word line enable signals WLEN1 to WLEN4 are obtained by decoding lower two bits of the row address signal and column address signal by the row decoder shown in FIG. 71.

(9) Row Decoder & Read Line Driver

[0719] A circuit example of the row decoder & read line driver used in Structural Example 9 (FIG. 59) will be described.

[0720] FIG. 73 shows a circuit example of the row decoder & read line driver. FIG. 73 shows the row decoder & read line driver of only one row.

[0721] The row decoder & read line driver 23B-1 is formed from an AND gate circuit AD9. The read signal READ and row address signal are input to the AND gate circuit AD9.

[0722] In the read operation, the read signal READ changes to "H". That is, in a mode except the read operation, the potential of the read word line RWL1 does not change to "H". In the read operation, in the selected row, all bits of the row address signal change to "H". Hence, the potential of the read line RWL1 is "H".

(10) Column Decoder & Write Bit Line Driver/Sinker

[0723] FIG. 74 is a circuit diagram showing a magnetic random access memory according to Structural Example 11 of the present invention.

[0724] Structural Example 11 has a characteristic that the write word lines WWLj are extended in column direction and the write bit lines WBL4(n-1)+1,···4(n-1)+4 are extended in row direction.

[0725] A circuit example of the column decoder & write bit line driver/sinker used in Structural Example 11 will be described.

[0726] FIGS. 75 and 76 show a circuit example of the column decoder & write bit line driver/sinker.

[0727] FIGS. 75 and 76 show the column decoder & write bit line driver/sinker of only one column.

[0728] In this example, assume that a read block is formed from four MTJ elements, and the four MTJ elements in the Structural Example are selected by lower two bits CA0 and CA1 of the column address signal. In addition, a column of the memory cell array is selected by upper column address signal bits, i.e., a column address signal excluding its lower two bits CA0 and CA1.

[0729] The write bit line driver/sinker 29A is formed from the PMOS transistors QP5, QP6, QP7, and QP8, NMOS transistors QN5, QN6, QN7, and QN8, NAND gate circuits ND5, ND6, ND7, and ND8, AND gate circuits AD1, AD2, AD3, and AD4, and inverters INV1, INV2, INV3, and INV4.

[0730] The PMOS transistor QP5 is connected between the power supply terminal VDD and one end of the write bit line BL1. The output signal from the NAND gate circuit ND5 is supplied to the gate of the PMOS transistor QP5. The NMOS transistor QN5 is connected between one end of the write bit line BL1 and the ground terminal VSS. The output signal from the AND gate circuit AD1 is supplied to the gate of the NMOS transistor QN5.

[0731] The PMOS transistor QP6 is connected between the power supply terminal VDD and one end of the write bit line BL2. The output signal from the NAND gate circuit ND6 is supplied to the gate of the PMOS transistor QP6. The NMOS transistor QN6 is connected between one end of the write bit line BL2 and the ground terminal VSS. The output signal from the AND gate circuit AD2 is supplied to the gate of the NMOS transistor QN6.

[0732] The PMOS transistor QP7 is connected between the power supply terminal VDD and one end of the write bit line BL3. The output signal from the NAND gate circuit ND7 is supplied to the gate of the PMOS transistor QP7. The NMOS transistor QN7 is connected between one end of the write bit line BL3 and the ground terminal VSS. The output signal from the AND gate circuit AD3 is supplied to the gate of the NMOS transistor QN7.

[0733] The PMOS transistor QP8 is connected between the power supply terminal VDD and one end of the write bit line BL4. The output signal from the NAND gate circuit ND8 is supplied to the gate of the PMOS transistor QP8. The NMOS transistor QN8 is connected between one end of the write bit line BL4 and the ground terminal VSS. The output signal from the AND gate circuit AD4 is supplied to the gate of the NMOS transistor QN8.

[0734] The write bit line driver/sinker 31 is formed from the PMOS transistors QP9, QP10, QP11, and QP12, NMOS transistors QN9, QN10, QN11, and QN12, NAND gate circuits ND9, ND10, ND11, and

ND12, AND gate circuits AD5, AD6, AD7, and AD8, and inverters INV5, INV6, INV7, and INV8.

[0735] The PMOS transistor QP9 is connected between the power supply terminal VDD and the other end of the write bit line BL1. The output signal from the NAND gate circuit ND9 is supplied to the gate of the PMOS transistor QP9. The NMOS transistor QN9 is connected between the other end of the write bit line BL1 and the ground terminal VSS. The output signal from the AND gate circuit AD5 is supplied to the gate of the NMOS transistor QN9.

[0736] The PMOS transistor QP10 is connected between the power supply terminal VDD and the other end of the write bit line BL2. The output signal from the NAND gate circuit ND10 is supplied to the gate of the PMOS transistor QP10. The NMOS transistor QN10 is connected between the other end of the write bit line BL2 and the ground terminal VSS. The output signal from the AND gate circuit AD6 is supplied to the gate of the NMOS transistor QN10.

[0737] The PMOS transistor QP11 is connected between the power supply terminal VDD and the other end of the write bit line BL3. The output signal from the NAND gate circuit ND11 is supplied to the gate of the PMOS transistor QP11. The NMOS transistor QN11 is connected between the other end of the write bit line BL3 and the ground terminal VSS. The output signal from the AND gate circuit AD7 is supplied to the gate of the NMOS transistor QN11.

[0738] The PMOS transistor QP12 is connected between the power supply terminal VDD and the other end of the write bit line BL4. The output signal from the NAND gate circuit ND12 is supplied to the gate of the PMOS transistor QP12. The NMOS transistor QN12 is connected between the other end of the write bit line BL4 and the ground terminal VSS. The output signal from the AND gate circuit AD8 is supplied to the gate of the NMOS transistor QN12.

[0739] In the write bit line drivers/sinkers 29A and 31 with the above structures, when the output signal from the NAND gate circuit ND5 is "0", and the output signal from the AND gate circuit AD5 is "1", a write current from the write bit line driver/sinker 29A to the write bit line driver/sinker 31 flows to the write bit line BL1.

[0740] When the output signal from the NAND gate circuit ND9 is "0", and the output signal from the AND gate circuit AD1 is "1", a write current from the write bit line driver/sinker 31 to the write bit line driver/sinker 29A flows to the write bit line BL1.

[0741] When the output signal from the NAND gate circuit ND6 is "0", and the output signal from the AND gate circuit AD6 is "1", a write current from the write bit line driver/sinker 29A to the write bit line driver/sinker 31 flows to the write bit line BL2.

[0742] When the output signal from the NAND gate circuit ND10 is "0", and the output signal from the AND gate circuit AD2 is "1", a write current from the write bit line driver/sinker 31 to the write bit line driver/sinker 29A flows to the write bit line BL2.

[0743] When the output signal from the NAND gate circuit ND7 is "0", and the output signal from the AND gate circuit AD7 is "1", a write current from the write bit line driver/sinker 29A to the write bit line driver/sinker 31 flows to the write bit line BL3.

[0744] When the output signal from the NAND gate circuit ND11 is "0", and the output signal from the AND gate circuit AD3 is "1", a write current from the write bit line driver/sinker 31 to the write bit line driver/sinker 29A flows to the write bit line BL3.

[0745] When the output signal from the NAND gate circuit ND8 is "0", and the output signal from the AND gate circuit AD8 is "1", a write current from the write bit line driver/sinker 29A to the write bit line driver/sinker 31 flows to the write bit line BL4.

[0746] When the output signal from the NAND gate circuit ND12 is "0", and the output signal from the AND gate circuit AD4 is "1", a write current from the write bit line driver/sinker 31 to the write bit line driver/sinker 29A flows to the write bit line BL4.

[0747] In the write bit line drivers/sinkers 29A and 31, in the write operation, the write signal WRITE is "1". In the selected column, all bits of the upper column address signal, i.e., all bits of the column address signal excluding the lower two bits CAD and CA1 are "1".

[0748] The lower two bits CA0 and CA1 of the column address signal are signal bits for selecting one of the four write bit lines BL1, BL2, BL3, and BL4 in the selected column. A write current having a direction corresponding to the value of write data DATA flows to the selected write bit line.

[0749] The direction of write current flowing to the selected write bit line in the selected column is determined in accordance with the value of the write data DATA.

[0750] For example, when the write bit line BL1 is selected (CA0 = "0", and CA1 = "0"), and the write data DATA is "1", the output signal from the NAND gate circuit ND5 is "0". The output signal from the AND gate circuit AD5 is "1". As a result, a write current from the write bit line driver/sinker 29A to the write bit line driver/sinker 31 flows to the write bit line BL1.

[0751] Conversely, when the write data DATA is "0", the output signal from the NAND gate circuit ND9 is "0". The output signal from the AND gate circuit AD1 is "1". As a result, a write current from the write bit line driver/sinker 31 to the write bit line driver/sinker 29A flows to the write bit line BL1.

[0752] When the write bit line BL2 is selected (CA0 = "1", and CA1 = "0"), and the write data DATA is "1", the output signal from the NAND gate circuit ND6 is "0". The output signal from the AND gate circuit AD6 is "1". As a result, a write current from the write bit line driver/sinker 29A to the write bit line driver/sinker 31 flows to the write bit line BL2.

[0753] Conversely, when the write data DATA is "0", the output signal from the NAND gate circuit ND10 is "0". The output signal from the AND gate circuit AD2 is

"1". As a result, a write current from the write bit line driver/sinker 31 to the write bit line driver/sinker 29A flows to the write bit line BL2.

[0754] When the write bit line BL3 is selected (CA0 = "0", and CA1 = "1"), and the write data DATA is "1", the output signal from the NAND gate circuit ND7 is "0". The output signal from the AND gate circuit AD7 is "1". As a result, a write current from the write bit line driver/sinker 29A to the write bit line driver/sinker 31 flows to the write bit line BL3.

[0755] Conversely, when the write data DATA is "0", the output signal from the NAND gate circuit ND11 is "0". The output signal from the AND gate circuit AD3 is "1". As a result, a write current from the write bit line driver/sinker 31 to the write bit line driver/sinker 29A flows to the write bit line BL3.

[0756] When the write bit line BL4 is selected (CA0 = "1", and CA1 = "1"), and the write data DATA is "1", the output signal from the NAND gate circuit ND8 is "0". The output signal from the AND gate circuit AD8 is "1". As a result, a write current from the write bit line driver/sinker 29A to the write bit line driver/sinker 31 flows to the write bit line BL4.

[0757] Conversely, when the write data DATA is "0", the output signal from the NAND gate circuit ND12 is "0". The output signal from the AND gate circuit AD4 is "1". As a result, a write current from the write bit line driver/sinker 31 to the write bit line driver/sinker 29A flows to the write bit line BL4.

(11) Read Circuit

[0758] FIG. 77 shows a circuit example of the read circuit.

[0759] In this example, assume that four MTJ elements are arranged in a read block of one column, and the MTJ elements are independently connected to read bit lines. That is, four read bit lines are arranged in one column. These read bit lines are connected to the read circuit 29B through the column select switch.

[0760] The read circuit 29B of this example is applied to a 1-bit-type magnetic random access memory which outputs read data bits one by one.

[0761] Hence, the read circuit 29B has four sense amplifiers & bias circuits 29B11, 29B12, 29B13, and 29B14, a selector 29B2, and an output buffer 29B3.

[0762] In the read operation, read data are simultaneously read from four MTJ elements in the selected read block. These four read data are input to and sensed by the sense amplifiers & bias circuits 29B11, 29B12, 29B13, and 29B14, respectively.

[0763] On the basis of the lower two bits CA0 and CA1 of the column address signal, the selector 29B2 selects one of the four read data output from the sense amplifiers & bias circuits 29B11, 29B12, 29B13, and 29B14. The selected read data is output from the magnetic random access memory as output data through the output buffer 29B3.

[0764] This example assume that the read circuit 29B is applied to a 1-bit-type magnetic random access memory.

[0765] However, when the read circuit 29B is applied to, e.g., a 4-bit-type magnetic random access memory which outputs 4-bit read data, the selector 29B2 can be omitted. To the contrary, four output buffers 29B3 are required in correspondence with the sense amplifiers & bias circuits 29B11, 29B12, 29B13, and 29B14.

[0766] FIG. 78 shows a circuit example of the read circuit applied to a 4-bit-type magnetic random access memory.

[0767] The read circuit 29B has four sense amplifiers & bias circuits 29B11, 29B12, 29B13, and 29B14 and four output buffers 29B31, 29B32, 29B33, and 29B34.

[0768] In the read operation, read data are simultaneously read from four MTJ elements in the selected read block. These four read data are input to and sensed by the sense amplifiers & bias circuits 29B11, 29B12, 29B13, and 29B14, respectively.

[0769] The output data from the sense amplifiers & bias circuits 29B11, 29B12, 29B13, and 29B14 are output from the magnetic random access memory through the output buffers 29B31, 29B32, 29B33, and 29B34.

[0770] FIG. 79 shows a circuit example of the sense amplifier & bias circuit.

[0771] This sense amplifier & bias circuit corresponds to one of the four sense amplifiers & bias circuits shown in FIG. 77 or 78.

[0772] A sense amplifier S/A is formed from, e.g., a differential amplifier.

[0773] A PMOS transistor QP14 and NMOS transistor QN13 are connected in series between the power supply terminal VDD and the column select switch 29C. The negative input terminal of an operational amplifier OP is connected to a node n2. The output terminal of the operational amplifier OP is connected to the gate of the NMOS transistor QN13. A clamp potential VC is input to the positive input terminal of the operational amplifier OP.

[0774] The operational amplifier OP equalizes the potential of the node n2 with the clamp potential VC. The clamp potential VC is set to a predetermined positive value.

[0775] A constant current source Is1 generates a read current Iread. The read current Iread flows to a bit line BLi through a current mirror circuit formed from a PMOS transistor QP13 and the PMOS transistor QP14. The sense amplifier formed from, e.g., a differential amplifier senses the data of a memory cell (MTJ element) on the basis of the potential of a node n1 when the read current Iread is flowing.

[0776] FIG. 80 shows a circuit example of the sense amplifier. FIG. 81 shows a circuit example of the reference potential generating circuit of the sense amplifier.

[0777] The sense amplifier S/A is formed from, e.g., a differential amplifier. The sense amplifier S/A compares a potential Vn1 of the node n1 with a reference

potential Vref.

[0778] The reference potential Vref is generated by an MTJ element which stores "1" data and an MTJ element which stores "0" data.

[0779] A PMOS transistor QP16 and NMOS transistors QN14 and QN15 are connected in series between the power supply terminal VDD and the MTJ element which stores "1" data. A PMOS transistor QP17 and NMOS transistors QN16 and QN17 are connected in series between the power supply terminal VDD and the MTJ element which stores "0" data.

[0780] The drains of the PMOS transistors QP16 and QP17 are connected to each other. The drains of the NMOS transistors QN15 and QN17 are also connected to each other.

[0781] The operational amplifier OP equalizes the potential of a node n4 with the clamp potential VC. A constant current source Is2 generates the read current Iread. The read current Iread flows to the MTJ element which stores "1" data and MTJ element which stores "0" data through a current mirror circuit formed from the PMOS transistors QP15 and QP16.

[0782] The reference potential Vref is output from a node n3.

[0783] FIG. 82 shows a circuit example of the operational amplifier OP shown in FIGS. 79 and 81.

[0784] The operational amplifier OP is formed from PMOS transistors QP18 and QP19 and NMOS transistors QN18, QN19, and QN20. When an enable signal Enable changes to "H", the operational amplifier OP is set in an operative state.

[0785] FIG. 83 shows a circuit example of the sense amplifier & bias circuit.

[0786] This sense amplifier & bias circuit corresponds to one of the four sense amplifiers & bias circuits shown in FIGS. 77 and 78.

[0787] The sense amplifier & bias circuit of this example is applied to Structural Example 8 (FIG. 58).

[0788] When the sense amplifier & bias circuit is applied to Structural Example 8 (FIG. 58), NMOS transistors QN24 and QN25 in FIG. 83 have the same size as that of the column select switch CSW shown in FIG. 58. NMOS transistors QN20 and QN21 in FIG. 83 have the same size as that of the row select switch RSW2 shown in FIG. 58.

[0789] NMOS transistors QN17, QN18, and QN19 in FIG. 83 have the same size such that they have the same driving capability.

[0790] With this structure, the positive input potential of the operational amplifier is an almost intermediate potential between the negative input potential of the operational amplifier when "1" data is read out and that of the operational amplifier when "0" data is read out in FIG. 58. Hence, the positive input potential of the operational amplifier functions as a reference potential in the data read mode.

[0791] A signal VtA input to the gates of the NMOS transistors QN18 and QN19 equals the data discrimination voltage of the sense amplifier S/A. The read signal READ which changes to "H" in the read operation is input to the gates of the NMOS transistors QN20, QN21, QN24, and QN25.

[0792] Referring to FIG. 83, "1" indicates that the MTJ element stores "1" data, and "0" indicates that the MTJ element stores "0" data. VC equals the bias potential VC applied to the bias line 34 of Structural Example 8 (FIG. 58).

4. Write/Read Operation Principle

[0793] The write/read operation principle of the magnetic random access memory of the present invention will be described.

(1) Write Operation Principle

[0794] A write in MTJ elements is executed at random. For example, the row decoders 25-1,..., 25-n select one row on the basis of a row address signal. In the selected row, an output signal RLk from a row decoder 25-k changes to "H", so the row select switch RSW2 is turned on.

[0795] The column decoder & read column select line driver 32 is activated only in the read operation. Hence, all the read word lines RWL1,..., RWLj are in a floating state.

[0796] The write word line driver 23A selects one of the four MTJ elements in the selected read block BKik and, more specifically, one of the four write word lines WWL4(n-1)+1, WWL4(n-1)+2, WWL4(n-1)+3, and WWL(n-1)+4 on the basis of, e.g., the lower two bits CA0 and CA1 of the column address signal.

[0797] The write word line driver 23A supplies a write current to the selected write word line through the common data line (common driver line) 30 and row select switch RSW2.

[0798] The column decoders & write bit line drivers/sinkers 29A and 31 select a column on the basis of, e.g., upper column address signal bits (column address signal excluding the lower two bits CA0 and CA1) and supplies the write current to the write bit line WBLi in the selected column.

[0799] The column decoders & write bit line drivers/sinkers 29A and 31 determine the direction of write current to be supplied to the write bit line WBLi in the selected column in accordance with the value of write data.

[0800] The magnetizing direction of the free layer (storing layer) of the selected MTJ element is determined by the synthesized magnetic field generated by the write current flowing to the write word line and the write current flowing to the write bit line, and "1"/"0" information is stored in the MTJ element.

[0801] In this write operation principle, one terminal of the MTJ element is connected to the read word line RWLi in the floating state in the write operation. Hence, charges are injected into the read word line RWLi from

the write word lines WWL4(n-1)+1, WWL4(n-1)+2, WWL4(n-1)+3, and WWL(n-1)+4, though no potential difference is generated across the MTJ element.

[0802] Hence, even when the write word line and write bit line have different potentials at a predetermined portion in the write operation due to the interconnection resistance of the write word line and write bit line, no potential difference is generated across the MTJ element, and the tunneling barrier layer is not broken.

(2) Read Operation Principle

[0803] A read from MTJ elements is executed for each read block. For example, the row decoders 25-1,..., 25-n select one row on the basis of a row address signal. In the selected row, the output signal RLk from the row decoder 25-k changes to "H", so the row select switch RSW2 is turned on.

[0804] The column decoder & read column select line driver 32 selects a column on the basis of upper column address signal bits. In the selected column, the output signal from the column decoder & read column select line driver 32, i.e., the column select signal CSLi changes to "H", so the column select switch CSW is turned on.

[0805] That is, the potential of the read word line RWLi in the selected column is the ground potential VSS. The read word lines RWLi in the remaining unselected columns are set in the floating state.

[0806] In the read operation, the write word line driver 23A and column decoders & write bit line drivers/sinkers 29A and 31 are in an inoperative state.

[0807] The read circuit 29B generate, e.g., a read current. The read current flows to only the plurality of MTJ elements 12 in the read block which is present in the selected row and column.

[0808] More specifically, the read current is absorbed by the ground point VSS through the row select switches RSW2 in the selected row, the MTJ elements 12 in the read block, and the column select switch CSW in the selected column.

[0809] In the read operation, one terminal of each of the MTJ elements in read blocks that are present in the selected row and unselected columns is short-circuited. The read bit lines RBL4(n-1)+1, RBL4(n-1)+2, RBL4(n-1)+3, and RBL4(n-1)+4 in the selected row are short-circuited through the MTJ elements.

[0810] This problem can be solved by, in the read operation, fixing the potentials of the read bit lines RBL4(n-1)+1, RBL4(n-1)+2, RBL4(n-1)+3, and RBL4(n-1)+4 by a clamp circuit and detecting data on the basis of a change in amount of the read current.

[0811] The direction of read current is not particularly limited. The read current may flow in a direction in which the read current is absorbed by the read circuit 29B.

[0812] The change in amount of the read current flowing to the read bit lines RBL4(n-1)+1, RBL4(n-1)+2, RBL4(n-1)+3, and RBL4(n-1)+4 is detected by the sense amplifier in the read circuit 29B.

[0813] The data in each MTJ element is sensed by the sense amplifier in the read circuit 29B and then output from the magnetic random access memory. The data bits of the plurality of MTJ elements 12 in the read block may be output one by one or simultaneously.

[0814] To sequentially output the data bits of the plurality of MTJ elements one by one, one of the data of the plurality of MTJ elements 12 is selected using the lower column address signal bits CA0 and CA1.

(3) Structural Example 9 (FIG. 59)

① Write Operation Principle

[0815] The row decoders 25-1,..., 25-n select one row on the basis of a row address signal. In the selected row, the output signals WLEN1 to WLEN4 from the row decoder 25-k change to "H". Hence, the write word line driver 33-k is activated, and a write current is supplied to the write word lines WWL4(n-1)+1, WWL4(n-1)+2, WWL4(n-1)+3, and WWL(n-1)+4.

[0816] To write data in the MTJ elements at random, the lower two bits CA0 and CA1 of the column address signal, which select one of the four write word lines WWL4(n-1)+1, WWL4(n-1)+2, WWL4(n-1)+3, and WWL(n-1)+4, are input to the row decoders 25-1,..., 25-n, as shown in, e.g., FIG. 71.

[0817] That is, in Structural Example 9, four row decoders are arranged in one row, and different lower two bits CA0 and CA1 of column address signals are input to the row decoders, as shown in FIG. 71. In addition, the four word line enable lines WLEN1 to WLEN4 are arranged in one row such that the four write word lines WWL4(n-1)+1, WWL4(n-1)+2, WWL4(n-1)+3, and WWL(n-1)+4 can be independently driven.

[0818] The row decoders & read line drivers 23B-1,.., 23B-n and column decoder & read column select line driver 32 are activated only in the read operation.

[0819] For this reason, all the read word lines RWL1,..., RWLj are in the floating state, and the write word lines WWL4(n-1)+1, WWL4(n-1)+2, WWL4(n-1)+3, and WWL(n-1)+4 are electrically disconnected from the common data line 30.

[0820] The column decoders & write bit line drivers/sinkers 29A and 31 select a column on the basis of, e.g., upper column address signal bits (column address signal excluding the lower two bits CA0 and CA1) and supplies a write current to the write bit line WBLi in the selected column.

[0821] The column decoders & write bit line drivers/sinkers 29A and 31 determine the direction of write current to be supplied to the write bit line WBLi in the selected column in accordance with the value of write data.

[0822] The magnetizing direction of the free layer (storing layer) of the selected MTJ element is determined by the synthesized magnetic field generated by the write current flowing to the write word line and the write current flowing to the write bit line, and "1"/"0" in-

formation is stored in the MTJ element.

② Read Operation Principle

[0823] A read from MTJ elements is executed for each read block. In Structural Example 9, the row decoders 25-1,..., 25-n are in the inoperative state in the read operation. That is, all the output signals WLEN1 to WLEN4 from the row decoders 25-1,..., 25-n are "L".

[0824] The row decoders & read line drivers 23B-1,..., 23B-n select one row on the basis of the row address signal. In the selected row, the output signal from the row decoder & read line driver 23B-k, i.e., the potential of the read line RWk changes to "H", so the row select switch RSW2 is turned on.

[0825] The column decoder & read column select line driver 32 selects one column on the basis of upper column address signal bits. In the selected column, the output signal from the column decoder & read column select line driver 32, i.e., the column select signal CSLi changes to "H", so the column select switch CSW is turned on.

[0826] In the read operation, the write word line driver 33-k and column decoders & write bit line drivers/sinkers 29A and 31 are in the inoperative state.

[0827] The read circuit 29B generates, e.g., the read current. The read current flows to only the plurality of MTJ elements 12 in the read block which is present in the selected row and column.

[0828] More specifically, the read current is absorbed by the ground point VSS through the row select switches RSW2 in the selected row, the MTJ elements 12 in the read block, and the column select switch CSW in the selected column.

[0829] The direction of read current is not particularly limited. The read current may flow in a direction in which the read current is absorbed by the read circuit 29B.

5. Positional Relationship Between Pinning Layer and Storing Layer of Each MTJ Element

[0830] As in Structural Example 5 (e.g., the sectional view shown in FIG. 36), when MTJ elements are arranged on the upper and lower sides of a write line (write word line or write bit line), and data is to be written in the MTJ element on the upper or lower side of the write line using a magnetic field generated by a write current that flows to the write line, the positional relationship between the pinning layer (fixed layer) and the storing layer (free layer) or the magnetizing direction of the pinning layer in each MTJ element must be examined.

[0831] This is because the write operation principle or the write circuit arrangement changes depending on the direction of the current flowing to the write line.

(1) Positional Relationship Between Pinning Layer and Storing Layer of Each MTJ Element

[0832] As shown in FIG. 84, the positional relationship (relative relationship) between the pinning layer and the storing layer of each MTJ element (MTJ element) is preferably symmetrical with respect to a write line to be used.

[0833] For example, when MTJ elements are arranged on the upper and lower sides of a write line (write word line or write bit line), and data is to be written in the MTJ element on the upper or lower side of the write line using a magnetic field generated by a write current that flows to the write line, the positional relationship between the pinning layer and the storing layer of each MTJ element is set to be symmetrical with respect to the write line.

[0834] More specifically, assume that the MTJ element on the lower side of the write line has a storing layer on a side close to the write interconnection and a pinning layer on a side far from the write interconnection. In this case, the MTJ element on the upper side of the write line also has a storing layer on a side close to the write interconnection and a pinning layer on a side far from the write interconnection.

[0835] Similarly, assume that the MTJ element on the lower side of the write line has a pinning layer on a side close to the write interconnection and a storing layer on a side far from the write interconnection. In this case, the MTJ element on the upper side of the write line also has a pinning layer on a side close to the write interconnection and a storing layer on a side far from the write interconnection.

[0836] Note that this positional relationship is ensured for all MTJ elements in the memory cell array. In addition, for all write lines in the memory cell array, the MTJ element arranged on the upper side and that arranged on the lower side are symmetrically arranged.

[0837] With this positional relationship, the distance from a write line to a storing layer is substantially the same for all MTJ elements. That is, since the influence of a magnetic field generated by a write current flowing to a write line due to the write current flowing to the write line is the same for all MTJ elements. Hence, all MTJ elements can have the same write characteristic.

[0838] In this case, the direction of the MTJ element arranged on the lower (or upper) side of the write line is opposite to the direction of the MTJ element arranged on the upper (or lower) side of the write line.

[0839] However, that the directions of all the MTJ elements in the memory cell array are not the same, and, for example, the directions of the MTJ elements change for each stage is no disadvantage for the present invention (directions here include only two directions: upward and downward, and the semiconductor substrate side is defined as the lower side).

[0840] This is because in forming MTJ elements, the directions of the MTJ elements can easily be changed

only by changing the order of forming the layers of MTJ elements.

(2) Magnetizing Direction of Pinning Layer of MTJ Element

[0841] When MTJ elements are arranged on the upper and lower sides of a write line (write word line or write bit line), and data is to be written in the MTJ element on the upper or lower side of the write line using a magnetic field generated by a write current that flows to the write line, the write operation principle and read operation principle must be changed depending on the magnetizing direction of the pinning layer of the MTJ element.

[0842] This is because the direction of a magnetic field applied to an MTJ element arranged on the upper side of a write line is opposite to that of a magnetic field applied to an MTJ element arranged on the lower side of the write line even though the direction of a current that flows to the write line is constant.

① When Magnetizing Directions of Pinning Layers are Individually Set

[0843] When the magnetizing directions of pinning layers can be individually set, the magnetizing direction of the pinning layer of each MTJ element that is present on the lower side of a write line (write word line or write bit line) is made opposite to that of the pinning layer of each MTJ element that is present on the upper side of the write line. With this arrangement, the normal read operation principle and write operation principle can be applied.

[0844] That is, a state wherein the magnetizing direction of the pinning layer is the same as that of the storing layer can be defined as "1". A state wherein the magnetizing direction of the pinning layer is different from that of the storing layer can be defined as "0".

[0845] A detailed example will be described below.

[0846] As a presupposition, the axes of easy magnetization of the MTJ elements MTJ1-1 and MTJ1-2 are directed in the X-direction (a direction in which the write word lines run), as shown in FIGS. 85 and 86. In addition, the magnetizing direction of the pinning layer of the MTJ element MTJ1-1 arranged on the lower side of the write bit line WBL1-1/WBL1-2 is leftward. The magnetizing direction of the pinning layer of the MTJ element MTJ1-2 arranged on the upper side of the write bit line WBL1-1/WBL1-2 is rightward.

[0847] Furthermore, write data is determined by the direction of a write current flowing to the write bit line WBL1-1/WBL1-2. Only a write current directed in one direction flows to the write word lines WWL1-1 and WWL1-2.

· When Data Is to Be Written in MTJ Element on Lower Side of Write Bit Line

["1"-Write]

[0848] As shown in FIG. 85, a write current directed in one direction is supplied to the write word line WWL1-1. A write current is supplied to the write bit line WBL1-1/WBL1-2 in a direction in which the current is absorbed in the direction perpendicular to the drawing surface. A magnetic field generated by the write current flowing to the write bit line WBL1-1/WBL1-2 forms a circle clockwise about the write bit line WBL1-1/WBL1-2.

[0849] In this case, a leftward magnetic field is applied to the MTJ element MTJ1-1 on the lower side of the write bit line WBL1-1/WBL1-2. For this reason, the magnetizing direction of the MTJ element MTJ1-1 on the lower side of the write bit line WBL1-1/WBL1-2 is leftward.

[0850] Hence, the magnetizing state of the MTJ element MTJ1-1 on the lower side of the write bit line WBL1-1/WBL1-2 is parallel, and data "1" is written.

["0"-Write]

[0851] A write current directed in one direction is supplied to the write word line WWL1-1. A write current is supplied to the write bit line WBL1-1/WBL1-2 in a direction in which the current comes out from the direction perpendicular to the drawing surface. A magnetic field generated by the write current flowing to the write bit line WBL1-1/WBL1-2 forms a circle counterclockwise about the write bit line WBL1-1/WBL1-2.

[0852] In this case, a rightward magnetic field is applied to the MTJ element MTJ1-1 on the lower side of the write bit line WBL1-1/WBL1-2. For this reason, the magnetizing direction of the MTJ element MTJ1-1 on the lower side of the write bit line WBL1-1/WBL1-2 is rightward.

[0853] Hence, the magnetizing state of the MTJ element MTJ1-1 on the lower side of the write bit line WBL1-1/WBL1-2 is antiparallel, and data "0" is written.

· When Data Is to Be Written in MTJ Element on Upper Side of Write Bit Line

[0854] If the same data can be written in the MTJ element MTJ1-2 on the upper side of the write bit line WBL1-1/WBL1-2 under the same write condition as for the MTJ element MTJ1-1, the write and read operations can be executed for the two MTJ elements MTJ1-1 and MTJ1-2 using the same write circuit (write bit line driver/sinker) and same read circuit.

["1"-Write]

[0855] As shown in FIG. 86, a write current directed in one direction is supplied to the write word line WWL1-2. A write current is supplied to the write bit line WBL1-1/WBL1-2 in a direction in which the current is absorbed in the direction perpendicular to the drawing

surface.

[0856] This write condition is the same as the "1"-write condition for the MTJ element MTJ1-1 on the lower side of the write bit line WBL1-1/WBL1-2. At this time, a magnetic field generated by the write current flowing to the write bit line WBL1-1/WBL1-2 forms a circle clockwise about the write bit line WBL1-1/WBL1-2.

[0857] In this case, a rightward magnetic field is applied to the MTJ element MTJ1-2 on the upper side of the write bit line WBL1-1/WBL1-2. For this reason, the magnetizing direction of the MTJ element MTJ1-2 on the upper side of the write bit line WBL1-1/WBL1-2 is rightward.

[0858] Hence, the magnetizing state of the MTJ element MTJ1-2 on the upper side of the write bit line WBL1-1/WBL1-2 is parallel, and data "1" is written.

[0859] As described above, when the magnetizing directions of the pinning layers of the MTJ elements MTJ1-1 and MTJ1-2 are opposite to each other, the same data can be written in the MTJ elements MTJ1-1 and MTJ1-2 under the same write condition.

["0"-Write]

[0860] A write current directed in one direction is supplied to the write word line WWL1-2. A write current is supplied to the write bit line WBL1-1/WBL1-2 in a direction in which the current comes out from the direction perpendicular to the drawing surface.

[0861] This write condition is the same as the "0"-write condition for the MTJ element MTJ1-1 on the lower side of the write bit line WBL1-1/WBL1-2. At this time, a magnetic field generated by the write current flowing to the write bit line WBL1-1/WBL1-2 forms a circle counterclockwise about the write bit line WBL1-1/WBL1-2.

[0862] In this case, a leftward magnetic field is applied to the MTJ element MTJ1-2 on the upper side of the write bit line WBL1-1/WBL1-2. For this reason, the magnetizing direction of the MTJ element MTJ1-2 on the upper side of the write bit line WBL1-1/WBL1-2 is leftward.

[0863] Hence, the magnetizing state of the MTJ element MTJ1-2 on the upper side of the write bit line WBL1-1/WBL1-2 is antiparallel, and data "0" is written.

[0864] As described above, when the magnetizing directions of the pinning layers of the MTJ elements MTJ1-1 and MTJ1-2 are opposite to each other, the same data can be written in the MTJ elements MTJ1-1 and MTJ1-2 under the same write condition.

② When Pinning Layers of All MTJ Elements Have Same Magnetizing Direction

[0865] When the pinning layers of all the MTJ elements have the same magnetizing direction, for example, after the wafer process is ended, the magnetizing direction of the pinning layers of all the MTJ elements can be instantaneously determined by simultaneously applying magnetic fields in the same direction to the pinning layers of all the MTJ elements.

[0866] Especially, when the temperature of the wafer is increased in applying the magnetic field, the magnetizing directions of the pinning layers of all the MTJ elements can easily be determined.

[0867] In this case, however, identical data cannot be written in the MTJ elements arranged on the lower side of a write line and MTJ elements arranged on the upper side of the write line under the same condition.

[0868] The following two countermeasures can be used: A. the arrangement of the read circuit is changed without changing the arrangement of the write circuit (write bit line driver/sinker), i.e., the write condition, and B. the arrangement of the write circuit (write bit line driver/sinker), i.e., the write condition is changed without changing the arrangement of the read circuit.

[0869] A detailed example will be described below.

[0870] As a presupposition, the axes of easy magnetization of the MTJ elements MTJ1-1 and MTJ1-2 are directed in the X-direction (a direction in which the write word lines run), as shown in FIGS. 87 and 88. In addition, both the magnetizing direction of the pinning layer of the MTJ element MTJ1-1 arranged on the lower side of the write bit line WBL1-1/WBL1-2 and the magnetizing direction of the pinning layer of the MTJ element MTJ1-2 arranged on the upper side of the write bit line WBL1-1/WBL1-2 are leftward.

[0871] Furthermore, write data is determined by the direction of a write current flowing to the write bit line WBL1-1/WBL1-2. Only a write current directed in one direction flows to the write word lines WWL1-1 and WWL1-2.

A. When Write Condition Is Not Changed

· When Data Is to Be Written in MTJ Element on Lower Side of Write Bit Line

["1"-Write]

[0872] As shown in FIG. 87, a write current directed in one direction is supplied to the write word line WWL1-1. A write current is supplied to the write bit line WBL1-1/WBL1-2 in a direction in which the current is absorbed in the direction perpendicular to the drawing surface. A magnetic field generated by the write current flowing to the write bit line WBL1-1/WBL1-2 forms a circle clockwise about the write bit line WBL1-1/WBL1-2.

[0873] In this case, a leftward magnetic field is applied to the MTJ element MTJ1-1 on the lower side of the write bit line WBL1-1/WBL1-2. For this reason, the magnetizing direction of the MTJ element MTJ1-1 on the lower side of the write bit line WBL1-1/WBL1-2 is leftward.

[0874] Hence, the magnetizing state of the MTJ element MTJ1-1 on the lower side of the write bit line WBL1-1/WBL1-2 is parallel, and data "1" is written.

["0"-Write]

[0875] A write current directed in one direction is supplied to the write word line WWL1-1. A write current is supplied to the write bit line WBL1-1/WBL1-2 in a direction in which the current comes out from the direction perpendicular to the drawing surface. A magnetic field generated by the write current flowing to the write bit line WBL1-1/WBL1-2 forms a circle counterclockwise about the write bit line WBL1-1/WBL1-2.

[0876] In this case, a rightward magnetic field is applied to the MTJ element MTJ1-1 on the lower side of the write bit line WBL1-1/WBL1-2. For this reason, the magnetizing direction of the MTJ element MTJ1-1 on the lower side of the write bit line WBL1-1/WBL1-2 is rightward.

[0877] Hence, the magnetizing state of the MTJ element MTJ1-1 on the lower side of the write bit line WBL1-1/WBL1-2 is antiparallel, and data "0" is written.

· When Data Is to Be Written in MTJ Element on Upper Side of Write Bit Line

[0878] For the MTJ element MTJ1-2 on the upper side of the write bit line WBL1-1/WBL1-2, the write operation is executed using the same write condition, i.e., the same write circuit (write bit line driver/sinker) as that for the MTJ element MTJ1-1.

["1"-Write]

[0879] As shown in FIG. 88, a write current directed in one direction is supplied to the write word line WWL1-2. A write current is supplied to the write bit line WBL1-1/WBL1-2 in a direction in which the current is absorbed in the direction perpendicular to the drawing surface.

[0880] This write condition is the same as the "1"-write condition for the MTJ element MTJ1-1 on the lower side of the write bit line WBL1-1/WBL1-2. At this time, a magnetic field generated by the write current flowing to the write bit line WBL1-1/WBL1-2 forms a circle clockwise about the write bit line WBL1-1/WBL1-2.

[0881] In this case, a rightward magnetic field is applied to the MTJ element MTJ1-2 on the upper side of the write bit line WBL1-1/WBL1-2. For this reason, the magnetizing direction of the MTJ element MTJ1-2 on the upper side of the write bit line WBL1-1/WBL1-2 is rightward.

[0882] Hence, the magnetizing state of the MTJ element MTJ1-2 on the upper side of the write bit line WBL1-1/WBL1-2 is antiparallel, i.e., data "0" is stored.

[0883] The write data for the MTJ element MTJ1-2 is "1". Hence, in the read mode, the "0"-data stored in the MTJ element MTJ1-2 must be read out not as "0" but as "1".

[0884] To do this, the arrangement of the read circuit is slightly changed.

[0885] Basically, since write data in an inverted state is stored in the MTJ element that is present on the upper side of the write bit line, one inverter is added to the output section (final stage) of the read circuit for reading the data of the MTJ element that is present on the upper side of the write bit line.

[0886] For example, in Structural Example 5 (FIG. 36), the write bit line WBL1-1/WBL1-2 is arranged between the MTJ element MTJ1-1 of the first stage and the MTJ element MTJ1-2 of the second stage. For example, when the so-called batch read operation principle is applied, one inverter is added to each of the output sections of the logic circuits for discriminating data.

[0887] When the pinning layers of the MTJ elements MTJ1-1 and MTJ1-2 have the same magnetizing direction, data opposite to write data is stored in one of the MTJ element arranged on the upper side of the write line and that arranged on the lower side of the write line.

[0888] Hence, when one inverter is added to the output section (final stage) of the read circuit for reading the data of the MTJ element that stores opposite data, the write operation can be executed without changing the arrangement of the write circuit (write bit line driver/sinker).

["0"-Write]

[0889] A write current directed in one direction is supplied to the write word line WWL1-2. A write current is supplied to the write bit line WBL1-1/WBL1-2 in a direction in which the current comes out from the direction perpendicular to the drawing surface.

[0890] This write condition is the same as the "0"-write condition for the MTJ element MTJ1-1 on the lower side of the write bit line WBL1-1/WBL1-2. At this time, a magnetic field generated by the write current flowing to the write bit line WBL1-1/WBL1-2 forms a circle counterclockwise about the write bit line WBL1-1/WBL1-2.

[0891] In this case, a leftward magnetic field is applied to the MTJ element MTJ1-2 on the upper side of the write bit line WBL1-1/WBL1-2. For this reason, the magnetizing direction of the MTJ element MTJ1-2 on the upper side of the write bit line WBL1-1/WBL1-2 is leftward.

[0892] Hence, the magnetizing state of the MTJ element MTJ1-2 on the upper side of the write bit line WBL1-1/WBL1-2 is parallel, i.e., data "1" is stored.

[0893] The write data for the MTJ element MTJ1-2 is "0". Hence, in the read mode, the "1"-data stored in the MTJ element MTJ1-2 must be read out not as "1" but as "0".

[0894] When one inverter is added to the output section (final stage) of the read circuit for reading the data of the MTJ element that is present on the upper side of the write bit line, as described above, the data can be read without any problem.

B. When Write Condition Is Changed

[0895] When the write condition is changed, both the states of the MTJ elements MTJ1-1 and MTJ1-2 can be

set to parallel when the write data is "1". When the write data is "0", both the states of the MTJ elements MTJ1-1 and MTJ1-2 can be set to antiparallel.

[0896] That is, the read circuit need not be changed.

· When Data Is to Be Written in MTJ Element on Lower Side of Write Bit Line

["1"-Write]

[0897] As shown in FIG. 87, a write current directed in one direction is supplied to the write word line WWL1-1. A write current is supplied to the write bit line WBL1-1/WBL1-2 in a direction in which the current is absorbed in the direction perpendicular to the drawing surface. A magnetic field generated by the write current flowing to the write bit line WBL1-1/WBL1-2 forms a circle clockwise about the write bit line WBL1-1/WBL1-2.

[0898] In this case, a leftward magnetic field is applied to the MTJ element MTJ1-1 on the lower side of the write bit line WBL1-1/WBL1-2. For this reason, the magnetizing direction of the MTJ element MTJ1-1 on the lower side of the write bit line WBL1-1/WBL1-2 is leftward.

[0899] Hence, the magnetizing state of the MTJ element MTJ1-1 on the lower side of the write bit line WBL1-1/WBL1-2 is parallel, and data "1" is written.

["0"-Write]

[0900] A write current directed in one direction is supplied to the write word line WWL1-1. A write current is supplied to the write bit line WBL1-1/WBL1-2 in a direction in which the current comes out from the direction perpendicular to the drawing surface. A magnetic field generated by the write current flowing to the write bit line WBL1-1/WBL1-2 forms a circle counterclockwise about the write bit line WBL1-1/WBL1-2.

[0901] In this case, a rightward magnetic field is applied to the MTJ element MTJ1-1 on the lower side of the write bit line WBL1-1/WBL1-2. For this reason, the magnetizing direction of the MTJ element MTJ1-1 on the lower side of the write bit line WBL1-1/WBL1-2 is rightward.

[0902] Hence, the magnetizing state of the MTJ element MTJ1-1 on the lower side of the write bit line WBL1-1/WBL1-2 is antiparallel, and data "0" is written.

· When Data Is to Be Written in MTJ Element on Upper Side of Write Bit Line

["1"-Write]

[0903] As shown in FIG. 89, a write current directed in one direction is supplied to the write word line WWL1-2. A write current is supplied to the write bit line WBL1-1/WBL1-2 in a direction in which the current comes out from the direction perpendicular to the drawing surface.

[0904] This write condition is different from the "1"-write condition for the MTJ element MTJ1-1 on the lower side of the write bit line WBL1-1/WBL1-2. That is, if the write data is the same, the direction of the write current to be supplied to the write line changes depending on whether the MTJ element is present on the upper or lower side of the write line.

[0905] A write circuit (write bit line driver/sinker) which realizes such operation will be described later.

[0906] At this time, a magnetic field generated by the write current flowing to the write bit line WBL1-1/WBL1-2 forms a circle counterclockwise about the write bit line WBL1-1/WBL1-2.

[0907] In this case, a leftward magnetic field is applied to the MTJ element MTJ1-2 on the upper side of the write bit line WBL1-1/WBL1-2. For this reason, the magnetizing direction of the MTJ element MTJ1-2 on the upper side of the write bit line WBL1-1/WBL1-2 is leftward.

[0908] Hence, the magnetizing state of the MTJ element MTJ1-2 on the upper side of the write bit line WBL1-1/WBL1-2 is parallel, i.e., data "1" is stored.

["0"-Write]

[0909] A write current directed in one direction is supplied to the write word line WWL1-2. A write current is supplied to the write bit line WBL1-1/WBL1-2 in a direction in which the current is absorbed in the direction perpendicular to the drawing surface.

[0910] This write condition is different from the "0"-write condition for the MTJ element MTJ1-1 on the lower side of the write bit line WBL1-1/WBL1-2. That is, if the write data is the same, the direction of the write current to be supplied to the write line changes depending on whether the MTJ element is present on the upper or lower side of the write line.

[0911] At this time, a magnetic field generated by the write current flowing to the write bit line WBL1-1/WBL1-2 forms a circle clockwise about the write bit line WBL1-1/WBL1-2.

[0912] In this case, a rightward magnetic field is applied to the MTJ element MTJ1-2 on the upper side of the write bit line WBL1-1/WBL1-2. For this reason, the magnetizing direction of the MTJ element MTJ1-2 on the upper side of the write bit line WBL1-1/WBL1-2 is rightward.

[0913] Hence, the magnetizing state of the MTJ element MTJ1-2 on the upper side of the write bit line WBL1-1/WBL1-2 is antiparallel, i.e., data "0" is stored.

③ Arrangement of Write Circuit (Write Bit Line Driver/Sinker) When Pinning Layers of All MTJ Elements Have Same Magnetizing Direction

[0914] FIG. 90 shows a circuit example of the write bit line drivers/sinkers.

[0915] The circuit shown in FIG. 90 is applied to the magnetic random access memory according to Structural Example 5 (FIGS. 34 and 35). As a characteristic feature, this circuit has a function of changing the direc-

tion of write current on the basis of the position information (lower or upper side) of MTJ elements.

[0916] FIG. 90 shows write bit line drivers/sinkers corresponding to only one column.

[0917] The write bit line driver/sinker 29A is formed from the PMOS transistor QP1, NMOS transistor QN1, NAND gate circuit ND1, AND gate circuit AD1, exclusive OR circuit Ex-OR1, and exclusive NOR circuit Ex-NOR1.

[0918] The write bit line driver/sinker 31 is formed from the PMOS transistor QP2, NMOS transistor QN2, NAND gate circuit ND2, AND gate circuit AD2, exclusive OR circuit Ex-OR2, and exclusive NOR circuit Ex-NOR2.

[0919] The PMOS transistor QP1 is connected between the power supply terminal VDD and the write bit line WBL1-1/WBL1-2. The NMOS transistor QN1 is connected between the write bit line WBL1-1/WBL1-2 and the ground terminal VSS. The PMOS transistor QP2 is connected between the power supply terminal VDD and the write bit line WBL1-1/WBL1-2. The NMOS transistor QN2 is connected between the write bit line WBL1-1/WBL1-2 and the ground terminal VSS.

[0920] When the output signal from the NAND gate circuit ND1 is "0", and the output signal from the AND gate circuit AD2 is "1", a write current from the write bit line driver/sinker 29A toward the write bit line driver/sinker 31 flows to the write bit line WBL1-1/WBL1-2.

[0921] When the output signal from the NAND gate circuit ND2 is "0", and the output signal from the AND gate circuit AD1 is "1", a write current from the write bit line driver/sinker 31 toward the write bit line driver/sinker 29A flows to the write bit line WBL1-1/WBL1-2.

[0922] In such write bit line drivers/sinkers 29A and 31, the write signal WRITE is "1" in the write operation. Additionally, in the selected column, all the upper column address signal bits are "1".

[0923] In this example, the direction of write current to be supplied to the write bit line WBL1-1/WBL1-2 is determined using a select signal ZA0 for selecting a memory cell array (upper or lower stage).

· When Write Data Is "1"

[0924] When write data is "1" (DATA = "1"), the direction of current flowing to the write bit line WBL1-1/WBL1-2 is as follows.

[0925] When the memory cell array (MTJ elements) of the first stage is selected, ZA0 = "0". The output signals from the exclusive OR circuits Ex-OR1 and Ex-OR2 are "1", and the output signals from the exclusive NOR circuits Ex-NOR1 and Ex-NOR2 are "0".

[0926] Hence, the output signal from the NAND gate circuit ND1 is "0", and the output signal from the AND gate circuit AD2 is "1". As a result, a write current from the write bit line driver/sinker 29A to the write bit line driver/sinker 31 flows to the write bit line WBL1-1/WBL1-2.

[0927] When the memory cell array (MTJ elements) of the second stage is selected, ZA0 = "1". The output signals from the exclusive OR circuits Ex-OR1 and Ex-OR2 are "0", and the output signals from the exclusive NOR circuits Ex-NOR1 and Ex-NOR2 are "1".

[0928] Hence, the output signal from the NAND gate circuit ND2 is "0", and the output signal from the AND gate circuit AD1 is "1". As a result, a write current from the write bit line driver/sinker 31 to the write bit line driver/sinker 29A flows to the write bit line WBL1-1/WBL1-2.

· When Write Data Is "0"

[0929] When write data is "0" (DATA = "0"), the direction of current flowing to the write bit line WBL1-1/WBL1-2 is as follows.

[0930] When the memory cell array (MTJ elements) of the first stage is selected, ZA0 = "0". The output signals from the exclusive OR circuits Ex-OR1 and Ex-OR2 are "0", and the output signals from the exclusive NOR circuits Ex-NOR1 and Ex-NOR2 are "1".

[0931] Hence, the output signal from the NAND gate circuit ND2 is "0", and the output signal from the AND gate circuit AD1 is "1". As a result, a write current from the write bit line driver/sinker 31 to the write bit line driver/sinker 29A flows to the write bit line WBL1-1/WBL1-2.

[0932] When the memory cell array (MTJ elements) of the second stage is selected, ZA0 = "1". The output signals from the exclusive OR circuits Ex-OR1 and Ex-OR2 are "1", and the output signals from the exclusive NOR circuits Ex-NOR1 and Ex-NOR2 are "0".

[0933] Hence, the output signal from the NAND gate circuit ND1 is "0", and the output signal from the AND gate circuit AD2 is "1". As a result, a write current from the write bit line driver/sinker 29A to the write bit line driver/sinker 31 flows to the write bit line WBL1-1/WBL1-2.

6. Manufacturing Method

[0934] The cell array structure, MTJ element structure, read circuit, and read operation principle of the magnetic random access memory of the present invention have been described above. Finally, a manufacturing method for implementing the magnetic random access memory of the present invention will be described.

[0935] The manufacturing method to be described below is related to Device Structure 2 of Structural Example 1. Device Structures 1 and 3 of Structural Example 1 and Structural Examples 2 to 10 can also easily be formed using the following manufacturing method.

(1) Cell Array Structure to be Manufactured

[0936] The cell array structure completed by the manufacturing method of the present invention will be briefly described first. Then, the manufacturing method of the cell array structure will be described.

[0937] FIG. 91 shows a cell array structure including the characteristic feature of Device Structure 2 of Structural Example 1.

[0938] Element isolation insulating layers 45 having an STI (Shallow Trench Isolation) structure are formed in the semiconductor substrate 41. Dummy interconnections 46 are formed on the element isolation insulating layers 45. The dummy interconnections 46 are formed in a periodical pattern (a repeat of a predetermined pattern) or a pattern uniform as a whole. In this example, the dummy interconnections 46 are arranged equidistantly.

[0939] The dummy interconnections 46 are made of the same material as that of interconnections of peripheral circuits arranged around the memory cell array, e. g., the gate interconnections of MOS transistors.

[0940] The read word line RWL1 running in the Y-direction is formed on the dummy interconnections 46. The four MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4 arrayed in the Y-direction are arranged on the read word line RWL1.

[0941] One terminal (upper end in this example) of each of the MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4 is commonly connected to the upper electrode 44. The contact plug 42 and conductive layer 43 electrically connect the upper electrode 44 to the read word line RWL1.

[0942] The contact portion between the upper electrode 44 and the read word line RWL1 is formed in the region between the MTJ elements MTJ1 and MTJ2 and the MTJ elements MTJ3 and MTJ4. When the MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4 are uniformly arranged to be symmetrical with respect to the contact portion, signal margin in the read operation due to the interconnection resistance or the like can be maximized.

[0943] The conductive layer 43 may be integrated with the upper electrode 44. That is, the conductive layer 43 and upper electrode 44 may be formed simultaneously using the same material.

[0944] The other terminal (lower end in this example) of each of the MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4 is electrically connected to a corresponding one of the read bit lines RBL1, RBL2, RBL3, and RBL4 (write word lines WWL1, WWL2, WWL3, and WWL4). The read bit lines RBL1, RBL2, RBL3, and RBL4 run in the X-direction (row direction).

[0945] The MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4 are independently connected to the read bit lines RBL1, RBL2, RBL3, and RBL4, respectively. That is, the four read bit lines RBL1, RBL2, RBL3, and RBL4 are arranged in correspondence with the four MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4.

[0946] The write bit line WBL1 is formed immediately on and near the MTJ elements MTJ1, MTJ2, MTJ3, and MTJ4. The write bit line WBL1 runs in the Y-direction.

(2) Steps in Manufacturing Method

[0947] The manufacturing method for implementing the cell array structure shown in FIG. 91 will be described below. A detailed manufacturing method (e.g., employment of a dual damascene process) will be described here. Hence, note that elements that are not illustrated in the cell array structure of FIG. 91 will be mentioned. However, the outline of the finally completed cell array structure is almost the same as that shown in FIG. 91.

[1] Element Isolation Step

[0948] First, as shown in FIG. 92, an element isolation insulating layer 52 having an STI (Shallow Trench Isolation) structure is formed in a semiconductor substrate 51.

[0949] The element isolation insulating layer 52 can be formed by, e.g., the following process.

[0950] A mask pattern (e.g., a silicon nitride film) is formed on the semiconductor substrate 51 by PEP (Photo Engraving Process). The semiconductor substrate 51 is etched by RIE (Reactive Ion Etching) using the mask pattern as a mask to form a trench in the semiconductor substrate 51. This trench is filled with an insulating layer (e.g., a silicon oxide layer) using, e.g., CVD (Chemical Vapor Deposition) and CMP (Chemical Mechanical Polishing).

[0951] After that, a p-type impurity (e.g., B or BF_2) or an n-type impurity (e.g., P or As) is doped into the semiconductor substrate by, e.g., ion implantation, as needed, to form a p-type well region or an n-type well region.

[2] MOSFET Forming Step

[0952] Next, as shown in FIG. 93, a MOS transistor functioning as a read select switch is formed on the surface region of the semiconductor substrate 51.

[0953] Dummy interconnections are formed in the memory cell array region simultaneously when the MOS transistor is formed (FIG. 95).

[0954] The MOS transistor can be formed by, e.g., the following process.

[0955] An impurity for controlling the threshold value of the MOS transistor is ion-implanted into the channel portion in the element region surrounded by the element isolation insulating layer 52. A gate insulating film (e.g., a silicon oxide film) 53 is formed in the element region by thermal oxidation. A gate electrode material (e.g., polysilicon containing an impurity) and cap insulating film (e.g., a silicon nitride film) 55 are formed on the gate insulating film 53 by CVD.

[0956] The cap insulating film 55 is patterned by PEP. Then, the gate electrode material and gate insulating film 53 are processed (etched) by RIE using the cap insulating film 55 as a mask. As a consequence, gate electrodes 54 running in the X-direction are formed on the

semiconductor substrate 51.

[0957] A p- or n-type impurity is doped into the semiconductor substrate 51 by ion implantation using the cap insulating film 55 and gate electrodes 54 as a mask. Lightly-doped impurity regions (LDD regions or extension regions) are formed in the semiconductor substrate.

[0958] An insulating film (e.g., a silicon nitride film) is formed on the entire surface of the semiconductor substrate 51 by CVD. After that, the insulating film is etched by RIE to form sidewall insulating layers 57 on the side surfaces of the gate electrodes 54 and cap insulating films 55. A p- or n-type impurity is doped into the semiconductor substrate 51 by ion implantation using the cap insulating films 55, gate electrodes 54, and sidewall insulating layers 57 as a mask. As a result, source regions 56A and drain regions 56B are formed in the semiconductor substrate 51.

[0959] After that, an interlayer dielectric film (e.g., a silicon oxide layer) 58 that completely covers the MOS transistor is formed on the entire surface of the semiconductor substrate 51 by CVD. In addition, the surface of the interlayer dielectric film 58 is planarized by CMP.

[3] Contact Hole Forming Step

[0960] Next, as shown in FIG. 94, contact holes 59 that reach the source regions 56A and drain regions 56B of MOS transistors are formed in the interlayer dielectric film 58 on the semiconductor substrate 51.

[0961] The contact holes 59 can easily be formed by, e.g., forming a resist pattern on the interlayer dielectric film 58 by PEP and etching the interlayer dielectric film 58 by RIE using the resist pattern as a mark. After etching, the resist pattern is removed.

[4] Interconnection Trench & First Interconnection Layer Forming Step

[0962] As shown in FIGS. 95 and 96, interconnection trenches 60 are formed in the interlayer dielectric film 58 on the semiconductor substrate 51. In the memory cell array region, the interconnection trenches 60 are trenches in which read word lines should be formed and run in, e.g., the Y-direction. The interconnection trenches 60 are indicated by broken lines in FIGS. 95 and 96.

[0963] The interconnection trenches 60 can easily be formed by, e.g., forming a resist pattern on the interlayer dielectric film 58 by PEP and etching the interlayer dielectric film 58 by RIE using the resist pattern as a mark. After etching, the resist pattern is removed.

[0964] As shown in FIGS. 96 and 97, a barrier metal layer (e.g., a multi-layer of Ti and TiN) 61 is formed on the interlayer dielectric film 58, the inner surfaces of the contact holes 59, and the inner surfaces of the interconnection trenches 60 by, e.g., sputtering. Subsequently, a metal layer (e.g., a W layer) 62 that completely fills the contact holes 59 and interconnection trenches 60 is formed on the barrier metal layer 61 by, e.g., sputtering.

[0965] After that, the metal layer 62 is polished by, e.g., CMP and left only in the contact holes 59 and interconnection trenches 60. The metal layer 62 remaining in each contact hole 59 forms a contact plug.

[0966] As shown in FIG. 98, the metal layer 62 remaining in each interconnection trench 60 forms a first interconnection layer (read word line).

[0967] As shown in FIG. 99, an interlayer dielectric film (e.g., a silicon oxide layer) 63 is formed on the interlayer dielectric film 58 by CVD.

[0968] The step comprising the contact hole forming step, the interconnection trench forming step, and the first interconnection layer forming step is called a dual damascene process.

[5] Interconnection Trench Forming Step

[0969] Next, as shown in FIG. 100, interconnection trenches 64 are formed in the interlayer dielectric film 63. In this example, the interconnection trenches 64 serve as trenches used to form write word lines (read bit lines) and run in the X-direction. Sidewall insulating layers (e.g., silicon nitride layers) for increasing the insulating function may be formed on the side surfaces of the interconnection trenches 64.

[0970] The interconnection trenches 64 can easily be formed by, e.g., forming a resist pattern on the interlayer dielectric film 63 by PEP and etching the interlayer dielectric film 63 by RIE using the resist pattern as a mask. After etching, the resist pattern is removed.

[0971] The sidewall insulating layers can easily be formed by forming an insulating film (e.g., a silicon nitride film) on the entire surface of the interlayer dielectric film 63 by CVD and etching the insulating film by RIE.

[6] Second Interconnection Layer Forming Step

[0972] Next, as shown in FIG. 101, a contact hole 65 that reaches the metal layer 62 serving as the read word line is formed in the interconnection trench 64.

[0973] The contact hole 65 can easily be formed by, e.g., forming a resist pattern on the interlayer dielectric film 63 by PEP and etching the interlayer dielectric film 63 by RIE using the resist pattern as a mask. After etching, the resist pattern is removed.

[0974] After that, a barrier metal layer (e.g., a multilayer of Ta and TaN) 66 is formed on the interlayer dielectric film 63 and the inner surfaces of the interconnection trenches 64 and contact hole 65 by, e.g., sputtering. Subsequently, a metal layer (e.g., a Cu layer) 67 that completely fills the interconnection trenches 64 and contact hole 65 is formed on the barrier metal layer 66 by, e.g., sputtering.

[0975] After that, the metal layer 67 is polished by, e.g., CMP and left only in the interconnection trenches 64 and contact hole 65. The metal layer 67 remaining in each interconnection trench 64 forms a second inter-

connection layer that functions as a write word line (read bit line). The metal layer 67 remaining in the contact hole 65 forms a contact plug.

[7] MTJ Element & Lower Electrode Forming Step

[0976] As shown in FIG. 102, a lower electrode (e.g., a Ta layer) 68 is formed on the interlayer dielectric film 63 by sputtering. Subsequently, a plurality of layers 69 for MTJ elements are formed on the lower electrode 68. The plurality of layers 69 include, e.g., a tunneling barrier layer, two ferromagnetic layers that sandwich the tunneling barrier layer, and an antiferromagnetic layer.

[0977] After that, as shown in FIG. 103, the plurality of layers 69 for MTJ elements are patterned to form a plurality of MTJ elements 69A on the lower electrode 68. Each of the e plurality of MTJ elements 69A finally has the structure shown in, e.g., FIG. 61, 62, or 63.

[0978] The plurality of layers 69 for MTJ elements can easily be patterned by forming a resist pattern on the plurality of layers 69 by PEP and etching the plurality of layers 69 by RIE using the resist pattern as a mask. After etching, the resist pattern is removed.

[0979] Subsequently, the lower electrode 68 for the MTJ elements is patterned.

[0980] The lower electrode 68 can easily be patterned by forming a resist pattern on the lower electrode 68 by PEP and etching the lower electrode 68 by RIE using the resist pattern as a mask. After etching, the resist pattern is removed.

[0981] After that, an interlayer dielectric film 70 that completely covers the MTJ elements 69A is formed by CVD. In addition, the interlayer dielectric film 70 is polished and planarized by CMP and left only between the MTJ elements 69A.

[8] Step of Forming Upper Electrode for MTJ Elements

[0982] As shown in FIG. 104, a contact hole that reaches the metal layer 67 serving as a contact plug is formed in the interlayer dielectric film 70.

[0983] The contact hole can easily be formed by, e.g., forming a resist pattern on the interlayer dielectric film 70 by PEP and etching the interlayer dielectric film 70 by RIE using the resist pattern as a mask. After etching, the resist pattern is removed.

[0984] After that, a metal layer (e.g., a Ta layer) 71 as the upper electrode for the MTJ elements 69A is formed on the MTJ elements 69A and interlayer dielectric film 70 by sputtering such that the contact hole is completely filled. In addition, the metal layer 71 is polished by CMP to planarize the surface of the metal layer 71.

[0985] The upper electrode 71 for the MTJ elements 69A is patterned.

[0986] The upper electrode 71 for the MTJ elements 69A can easily be patterned by, e.g., forming a resist pattern on the upper electrode 71 by PEP and etching the upper electrode 71 by RIE using the resist pattern as a mask. After etching, the resist pattern is removed.

[0987] With this patterning, the upper electrode 71 may be formed for each read block, as in Structural Example 1. Alternatively, the upper electrode 71 may be shared by read blocks in one column, as in Structural Example 10.

[9] Third Interconnection Layer Forming Step

[0988] Next, as shown in FIG. 105, an interlayer dielectric film 72 which completely covers the upper electrode 71 for the MTJ elements 69A is formed on the interlayer dielectric film 70 by CVD. In addition, the interlayer dielectric film 72 is polished by CMP to planarize the surface of the interlayer dielectric film 72.

[0989] Interconnection trenches are formed in the interlayer dielectric film 72. The interconnection trenches are trenches in which write bit lines are to be formed and run in the Y-direction. Sidewall insulating layers (e.g., silicon nitride layers) for increasing the insulating function may be formed on the side surfaces of the interconnection trenches.

[0990] The interconnection trenches can easily be formed by, e.g., forming a resist pattern on the interlayer dielectric film 72 by PEP and etching the interlayer dielectric film 72 by RIE using the resist pattern as a mask. After etching, the resist pattern is removed.

[0991] The sidewall insulating layers can easily be formed by forming an insulating film (e.g., a silicon nitride film) on the entire interlayer dielectric film 72 by CVD and etching the insulating layer by RIE.

[0992] After that, a barrier metal layer (e.g., a multilayer of Ta and TaN) 73 is formed on the interlayer dielectric film 72 and inner surfaces of the interconnection trenches by, e.g., sputtering. Subsequently, a metal layer (e.g., a Cu layer) 74 that completely fills the interconnection trenches is formed on the barrier metal layer 73 by, e.g., sputtering.

[0993] The metal layer 74 is polished by, e.g., CMP and left only in the interconnection trenches. The metal layer 74 remaining in each interconnection trench forms a third interconnection layer that functions as a write bit line.

[0994] FIG. 106 shows the final structure in which the upper electrode 71 is shared by read block in one column.

(3) Conclusion

[0995] According to this manufacturing method, a cell array structure in which no read select switch is connected between a read word line and one terminal of an MR element in a read block, and one of two write lines is not in contact with the MTJ element can be implemented.

[0996] No select switch (MOS transistor) is formed immediately under the MTJ element. Instead, for example, a plurality of dummy interconnections are equidistantly formed. For this reason, the interlayer dielectric film can

be planarized, and the characteristics of the MTJ element can be improved.

[0997] In this example, to form an interconnection layer, a damascene process and dual damascene process are employed. Instead, for example, a process of forming an interconnection layer by etching may be employed.

7. Others

[0998] Application examples of Structural Example 8 shown in FIG. 58 will be described briefly.

[0999] As a characteristic feature of the example shown in FIG. 58, the bias voltage VC is applied to the selected read word line RWLi in the read mode. The following modifications can also be made for the MRAM having this characteristic feature.

[1000] As a characteristic feature of an example shown in FIG. 108, the read circuit 29B is connected to the read word lines RWL1,..., RWLi. The column select switch CSW is connected between the read circuit 29B and the read word lines RWLi,..., RWLi. One bias circuit BIAS which generates the bias voltage VC is arranged in correspondence with one of the read word lines RWL1,..., RWLi. In the read operation, the row decoders 25-1,..., 25-n select one read bit line RBLi. The selected read bit line RBLi is connected to the ground point through the read bit line sinker 23A. All the remaining unselected read bit lines are set in the floating state.

[1001] An MRAM shown in FIG. 109 includes the characteristic feature of the MRAM shown in FIG. 108. As a characteristic feature of the example shown in FIG. 109, a plurality of read circuits 29B are present, and a plurality of bit data can simultaneously be read out from a plurality of memory cells (MTJ elements) by read operation of one cycle, unlike the example shown in FIG. 108.

[1002] An MRAM shown in FIG. 110 includes the characteristic feature of the MRAM shown in FIG. 108. As a characteristic feature of the example shown in FIG. 110, a plurality of read circuits 29B are present, and a plurality of bit data can simultaneously be read out from a plurality of memory cells (MTJ elements) by read operation of one cycle, unlike the example shown in FIG. 108.

[1003] In the above description, a MTJ element is used as a memory cell of the magnetic random access memory. However, even when the memory cell is formed from a GMR (Giant MagnetoResistance) element or CMR (Colossal MagnetoResistance) element, the present invention, i.e., various kinds of cell array structures, the read operation principle, and the detailed example of the read circuit can be applied.

[1004] The structure of a MTJ element, GMR element, or CMR element and the materials thereof are not particularly limited in applying the present invention. In this example, the number of MTJ elements in one read block is four. However, the number of MTJ elements in one read block is not limited to four and can freely be set.

[1005] As a switch element such as the row/column select switch of the magnetic random access memory, a bipolar transistor, diode, MIS (Metal Insulator Semiconductor) transistor (including a MOSFET), MES (Metal Semiconductor) transistor, or junction transistor can be used.

[1006] As has been described above, according to the present invention, a magnetic random access memory having a cell array structure which can implement an increase in memory capacity without forming any select switch in a read block and also prevent the MTJ elements from breaking in a write mode can be provided.

Claims

1. A magnetic random access memory comprising:

   a memory cell array (11) having memory cells (12) using a magnetoresistive effect;

   characterized by further comprising

   a first functional line (RWL1,···RWLj) which runs in a first direction in the memory cell array (11) and is commonly connected to one terminal of each of the memory cells (12);

   second functional lines (RBL4(n-1)+1, ···RBL4(n-1)+4, WWL4(n-1)+1, ···WWL4(n-1)+4) which are arranged in correspondence with the memory cells (12) and run in a second direction perpendicular to the first direction in the memory cell array (11); and

   a third functional line (WBL1,···WBLj) which is separated from the memory cells (12) and shared by the memory cells (12),

2. A memory according to claim 1, **characterized in that** the memory cell array (11) is arranged on a semiconductor substrate, and no switch element is present immediately under the memory cell array.

3. A memory according to claim 2, **characterized in that** dummy interconnections (54) which do not function as actual interconnections are arranged immediately under the memory cell array (11).

4. A memory according to claim 3, **characterized in that** each of the dummy interconnections (54) has the same structure as that of a gate electrode of a MOS transistor (53,54,56A,56B) arranged at a peripheral portion of the memory cell array (11).

5. A memory according to claim 3, **characterized in that** the dummy interconnections (54) are arranged equidistantly, periodically, or uniformly as a whole.

6. A memory according to claim 1, **characterized in**

that the memory cells (12) are arranged on a semiconductor substrate and arrayed in a direction parallel to a surface of the semiconductor substrate.

7. A memory according to claim 6, **characterized in that** the memory cells (12) are arrayed in the first direction, and the first and third functional lines run in the first direction in the memory cell array.

8. A memory according to claim 6, **characterized in that** when the memory cell array (11-1, ···11-n) and the first, second, and third functional lines (RWL1, ··· RWLj, RBL4(n-1)+1, ···RBL4(n-1)+4, WWL4(n-1)+1, ···WWL4(n-1)+4, WBL1, ···WBLj) form one memory cell unit, stages of memory cell units are stacked on the semiconductor substrate.

9. A memory according to claim 8, **characterized in that** for first and second memory cell units which are adjacent to each other in the memory cell units, the first functional line of the first memory cell unit and the third functional line of the second memory cell unit are integrated as a fourth functional line.

10. A memory according to claim 9, **characterized in that** the first memory cell unit is arranged on the second memory cell unit.

11. A memory according to claim 9, **characterized by** further comprising a switch circuit (22) which determines whether the fourth functional line should function as the first functional line of the first memory cell unit or the third functional line of the second memory cell unit.

12. A memory according to claim 9, **characterized in that** for first and second memory cell units which are adjacent to each other in the memory cell units, the first functional lines of the first and second memory cell units are integrated as a fifth functional line.

13. A memory according to claim 12, **characterized in that** for first and second memory cell units which are adjacent to each other in the memory cell units, the third functional lines of the first and second memory cell units are integrated as a sixth functional line.

14. A memory according to claim 13, **characterized in that** each of the memory cells of the first and second memory cell units is formed from a magnetic storage element having a pinning layer whose magnetizing direction is fixed, and the magnetizing direction of the pinning layer of each of the memory cells of the first memory cell unit is different from the magnetizing direction of the pinning layer of each of the memory cells of the second memory cell unit.

15. A memory according to claim 13, **characterized in that** each of the memory cells of the first and second memory cell units is formed from a magnetic storage element having a pinning layer whose magnetizing direction is fixed, and the pinning layers of the memory cells of the first and second memory cell units have the same magnetizing direction.

16. A memory according to claim 1, **characterized in that** the first functional line (RWL1, ···RWLj) and second functional lines (RBL4(n-1)+1, ···RBL4(n-1)+4, WWL4(n-1)+1, ···WWL4(n-1)+4) are arranged immediately under the memory cells, and the third functional line (WBL1, ···WBLj) is arranged immediately on the memory cells.

17. A memory according to claim 16, **characterized in that** said one terminal of each of the memory cells (MTJ1,MTJ2,MTJ3,MTJ4) corresponds to an upper surface of the memory cell, said other terminal of each of the memory cells corresponds to a lower surface of the memory cell, and the memory cells are arranged symmetrically with respect to the contact plug.

18. A memory according to claim 1, **characterized in that** the first functional line (RWL1, ···RWLj) and second functional lines (RBL4(n-1)+1, ···RBL4(n-1)+4, WWL4(n-1)+1, ···WWL4(n-1)+4) are arranged immediately on the memory cells, and the third functional line (WBL1,···WBLj) is arranged immediately under the memory cells.

19. A memory according to claim 18, **characterized in that** said one terminal of each of the memory cells (MTJ1,MTJ2,MTJ3,MTJ4) corresponds to a lower surface of the memory cell, said other terminal of each of the memory cells corresponds to an upper surface of the memory cell, and the memory cells are arranged symmetrically with respect to the contact plug.

20. A memory according to claim 17 or 19, **characterized in that** an electrode is connected to said one terminal of each of the memory cells, and said one terminal of each of the memory cells and the first functional line are connected through a contact plug.

21. A memory according to claim 1, **characterized in that** the first functional line (RWL1, ···RWLj) functions as a read line to supply a read current to the memory cells.

22. A memory according to claim 21, **characterized in that** one end of the first functional line is connected to a ground point through a column select switch.

23. A memory according to claim 21, **characterized in that** one end of the first functional line is connected to a bias line which is set to a bias potential.

24. A memory according to claim 1, **characterized in that** the second functional lines function as read lines to supply a read current to the memory cells and write lines which generate a magnetic field to write data in the memory cells.

25. A memory according to claim 24, **characterized in that** one end of each of the second functional lines is connected to a corresponding one of common lines arranged outside the memory cell array through a corresponding one of row select switches.

26. A memory according to claim 25, **characterized in that** the common lines run in the first direction.

27. A memory according to claim 25, **characterized in that** one end of each of the common lines is connected to a read circuit.

28. A memory according to claim 25, **characterized in that** one end of each of the common lines is connected to a driver, and the other end of each of the second functional lines is connected to a sinker.

29. A memory according to claim 25, **characterized in that** a driver is connected between the second functional lines and the row select switches, and a sinker is connected to the other end of each of the second functional lines.

30. A memory according to claim 28 or 29, **characterized in that** an axis of easy magnetization of the MTJ elements is set in the second direction.

31. A memory according to claim 24, **characterized in that** one end of each of the second functional lines is connected, through a corresponding one of first row select switches, to a corresponding one of first common lines arranged outside the memory cell array, and the other end of each of the second functional lines is connected, through a corresponding one of second row select switches, to a corresponding one of second common lines arranged outside the memory cell array.

32. A memory according to claim 31, **characterized in that** the first and second common lines run in the first direction.

33. A memory according to claim 31, **characterized in that** one end of each of the first common lines is connected to a read circuit.

34. A memory according to claim 31, **characterized in that** one end of each of the first common lines is connected to a first driver/sinker, and one end of each of the second common lines is connected to a second driver/sinker.

35. A memory according to claim 34, **characterized in that** an axis of easy magnetization of the MTJ elements is set in the first direction.

36. A memory according to claim 1, **characterized in that** the third functional line functions as a write line which generates a magnetic field to write data in the memory cells.

37. A memory according to claim 36, **characterized in that** drivers/sinkers are respectively connected to two ends of the third functional line.

38. A memory according to claim 36, **characterized in that** a driver is connected to one end of the third functional line, and a sinker is connected to the other end of the third functional line.

39. A memory according to claim 27 or 33, **characterized in that** the read circuit is formed from sense amplifiers which are arranged in correspondence with the second functional lines, and output buffers which are arranged in correspondence with the sense amplifiers.

40. A memory according to claim 27 or 33, **characterized in that** the read circuit is formed from sense amplifiers which are arranged in correspondence with the second functional lines, an output buffer which outputs data from one of the sense amplifiers, and a selector which is connected between the sense amplifiers and the output buffer.

41. A memory according to claim 39, **characterized in that** the sense amplifiers fix potentials of the second functional lines and detect a change in read current flowing through the second functional lines.

42. A memory according to claim 39, **characterized in that** the sense amplifiers fix potentials of the second functional lines and detect a change in read current flowing through the second functional lines.

43. A memory according to claim 1, **characterized in that** the memory cells form a read block, and data from the memory cells are simultaneously read out.

44. A memory according to claim 1, **characterized in that** each of the memory cells is formed from a magnetic storage element including a pinning layer whose magnetizing direction is fixed, a storing layer whose magnetizing direction changes in accord-

ance with write data, and a tunneling barrier layer arranged between the pinning layer and the storing layer.

45. A memory according to claim 1, **characterized in that** 2^n (n is a natural number) memory cells are present.

46. A memory according to claim 1, **characterized in that** each of the memory cells is formed from an element which stores data using a tunneling magnetoresistive effect.

47. A read method of a magnetic random access memory, **characterized by** comprising:

using the method to the magnetic random access memory of claim 1;
fixing all the second functional lines of claim 1 to a first potential;
setting the first functional line of claim 1 to a second potential different from the second potential;
individually supplying a read current to the memory cells of claim 1; and
reading out data from the memory cells on the basis of a value of the read current.

48. A write method of a magnetic random access memory, **characterized by** comprising:

using the method to the magnetic random access memory of claim 1;
supplying a first write current flowing in one direction to one of the second functional lines of claim 1;
supplying a second write current having a direction depending on write data to the third functional line of claim 1; and
writing the write data in one of the memory cells using a magnetic field generated by the first and second write currents.

49. A write method of a magnetic random access memory, **characterized by** comprising:

using the method to the magnetic random access memory of claim 1;
supplying a first write current having a direction depending on write data to one of the second functional lines of claim 1;
supplying a second write current flowing in one direction to the third functional line of claim 1; and
writing the write data in one of the memory cells using a magnetic field generated by the first and second write currents.

50. A manufacturing method of a magnetic random access memory, **characterized by** comprising:

a. forming a gate electrode of a MOS transistor in a peripheral circuit region and simultaneously forming, in a memory cell array region, dummy interconnections equidistantly, periodically, or in a layout uniform as a whole;
b. forming a first interlayer dielectric film which covers the MOS transistor and dummy interconnections;
c. forming a memory cell having a magnetoresistive effect in a surface region of the first interlayer dielectric film in the memory cell array region; and
d. forming a second interlayer dielectric film which covers the memory cell.

51. A method according to claim 50, **characterized in that** the same steps as the c. and d. steps are repeated after the d. step.

52. A method according to claim 50, **characterized by** further comprising:

e. forming a first functional line which is connected to one terminal of the memory cell and runs in a first direction;
f. forming a second functional line which is connected to the other terminal of the memory cell and runs in a second direction perpendicular to the first direction; and
g. forming a third functional line which is separated from the memory cell by a predetermined distance and generates a magnetic field to write data in the memory cell.

53. A method according to claim 50, **characterized in that** the first, second, and third functional lines are formed by a damascene process.

54. A method according to claim 50, **characterized in that** the first, second, and third functional lines are formed by steps of forming an interconnection trench, forming a metal layer which completely fills the interconnection trench, and removing the metal layer outside the interconnection trench.

55. A method according to claim 54, **characterized by** further comprising, before formation of the metal layer, a step of forming a barrier metal layer.

56. A method according to claim 55, **characterized by** further comprising

before formation of the barrier metal layer, forming a sidewall insulating layer on a sidewall of the interconnection trench, and

after removal of the metal layer outside the in-

terconnection trench, forming, only on the metal layer, a cap insulating layer made of the same material as that of the sidewall insulating layer.

57. A method according to claim 56, **characterized in that** the sidewall insulating layer and cap insulating layer are made of silicon nitride.

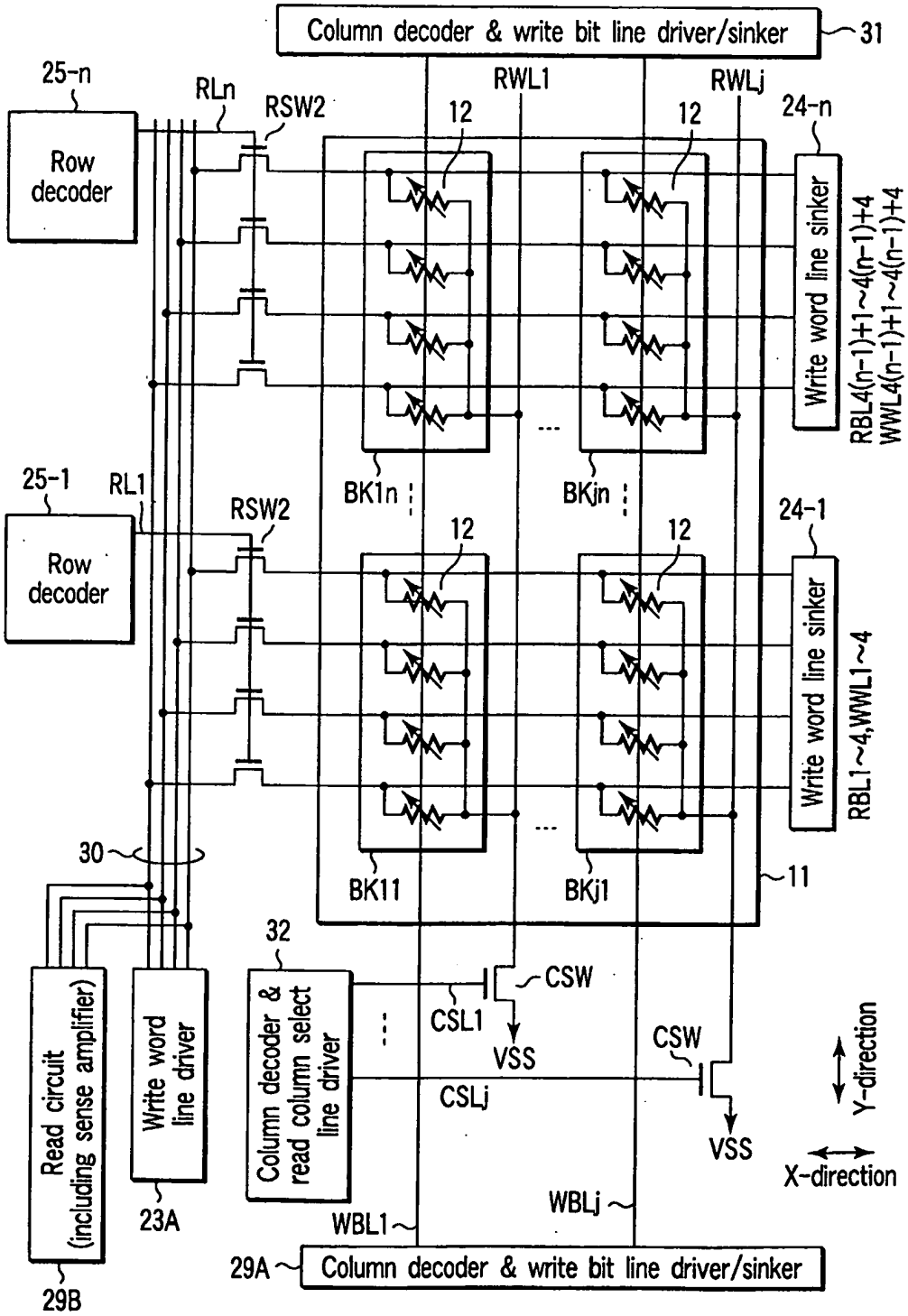
Column decoder & write bit line driver/sinker
31
25-n
Row decoder
RLn
RSW2
RWL1
RWLj
12
24-n
Write word line sinker
RBL4(n-1)+1~4(n-1)+4
WWL4(n-1)+1~4(n-1)+4
BK1n
BKjn
25-1
RL1
Row decoder
RSW2
24-1
Write word line sinker
RBL1~4,WWL1~4
30
BK11
BKj1
11
32
Read circuit (including sense amplifier)
Write word line driver
Column decoder & read column select line driver
CSW
CSL1
VSS
CSLj
Y-direction
X-direction
23A
WBL1
WBLj
29A
Column decoder & write bit line driver/sinker
29B

FIG. 1

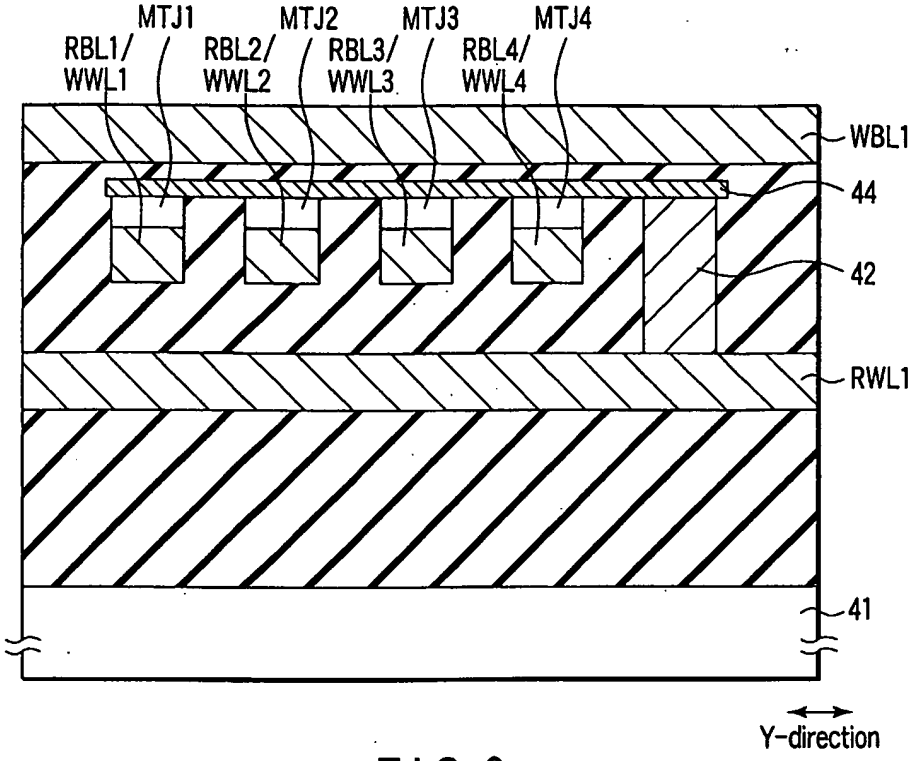
MTJ1
MTJ2
MTJ3
MTJ4
RBL1/
WWL1
RBL2/
WWL2
RBL3/
WWL3
RBL4/
WWL4
WBL1
44
42
RWL1
41
Y-direction

FIG. 2

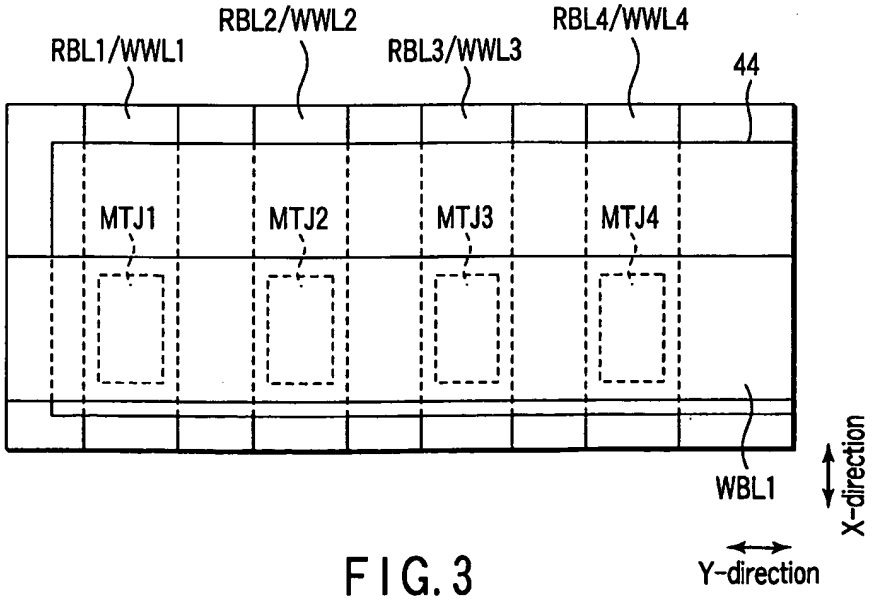
RBL1/WWL1
RBL2/WWL2
RBL3/WWL3
RBL4/WWL4
44
MTJ1
MTJ2
MTJ3
MTJ4
WBL1
X-direction
Y-direction

FIG. 3

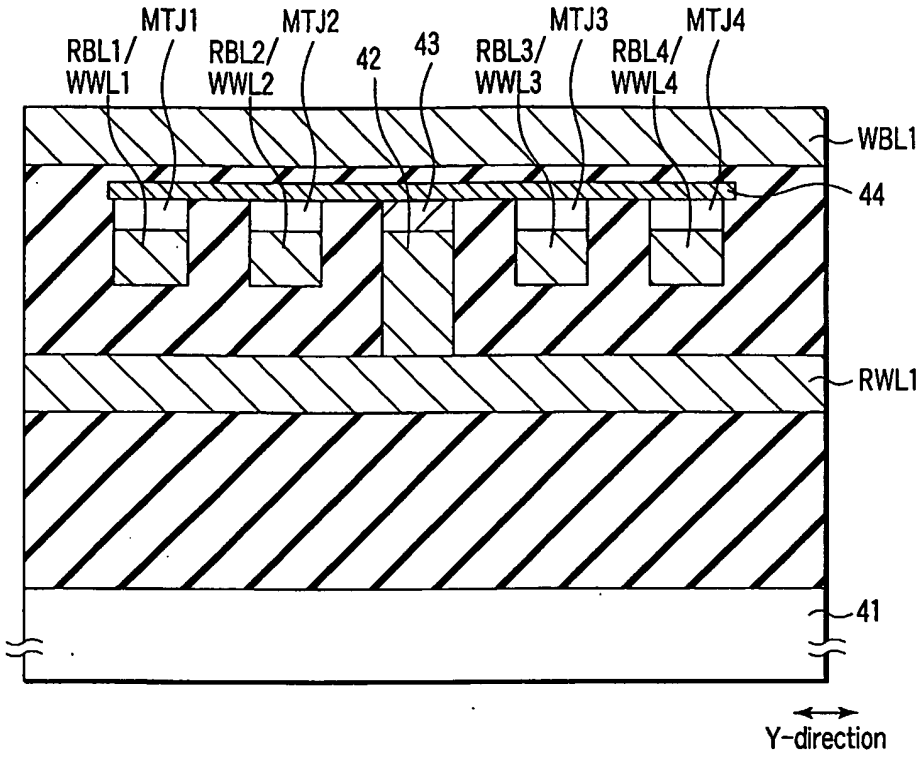
MTJ1
MTJ2
MTJ3
MTJ4
RBL1/
WWL1
RBL2/
WWL2
42
43
RBL3/
WWL3
RBL4/
WWL4
WBL1
44
RWL1
41
Y-direction

FIG. 4

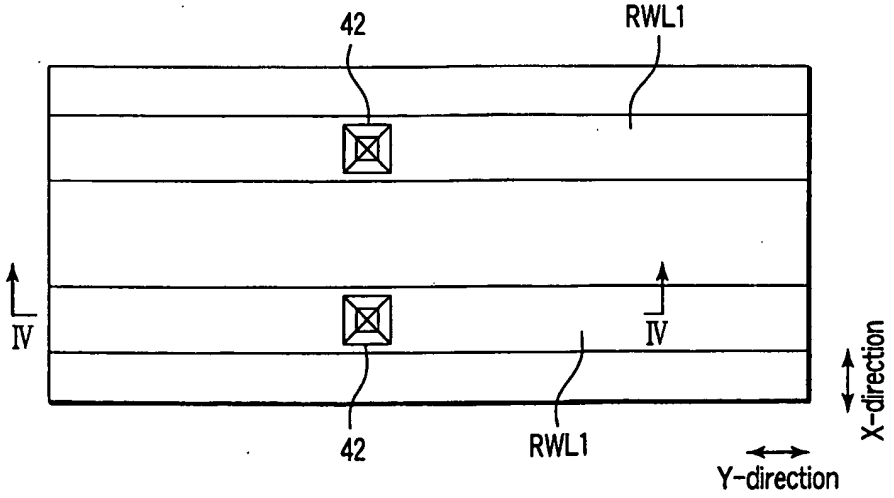
42
RWL1
IV
IV
42
RWL1
X-direction
Y-direction

FIG. 5

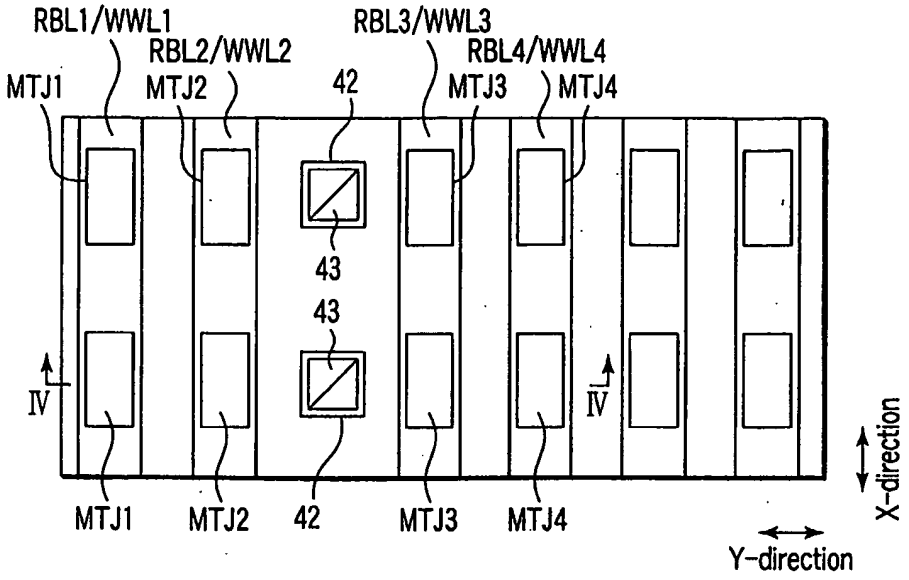
RBL1/WWL1
RBL2/WWL2
RBL3/WWL3
RBL4/WWL4
MTJ1
MTJ2
42
MTJ3
MTJ4
43
43
IV
IV
MTJ1
MTJ2
42
MTJ3
MTJ4
X-direction
Y-direction

FIG. 6

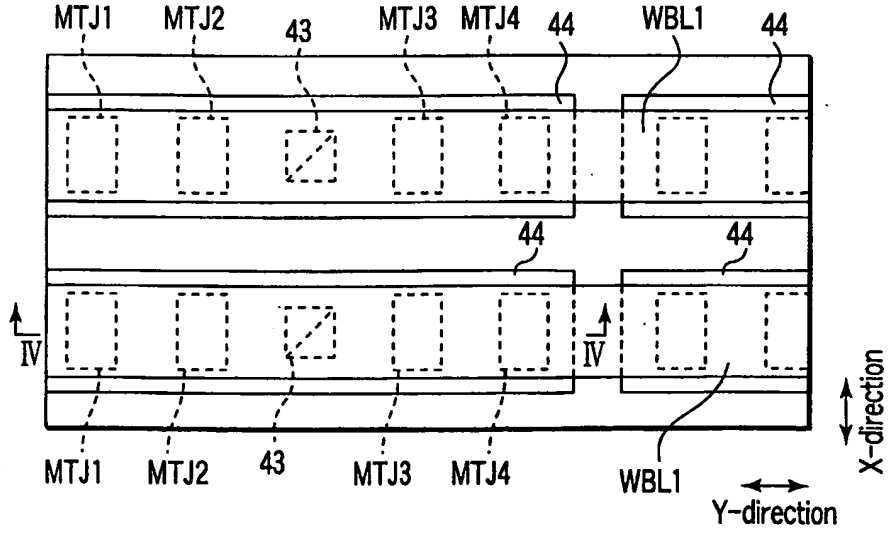
MTJ1
MTJ2
43
MTJ3
MTJ4
44
WBL1
44
44
44
IV
IV
MTJ1
MTJ2
43
MTJ3
MTJ4
WBL1
X-direction
Y-direction

FIG. 7

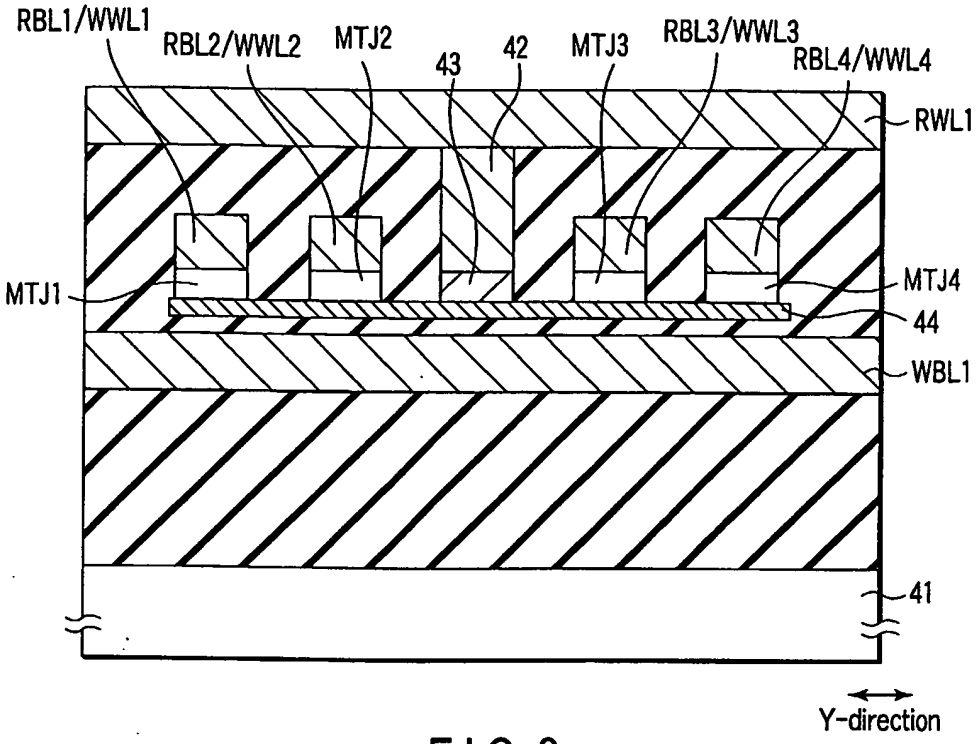
RBL1/WWL1
RBL2/WWL2
MTJ2
43
42
MTJ3
RBL3/WWL3
RBL4/WWL4
RWL1
MTJ1
MTJ4
44
WBL1
41
Y-direction

FIG. 8

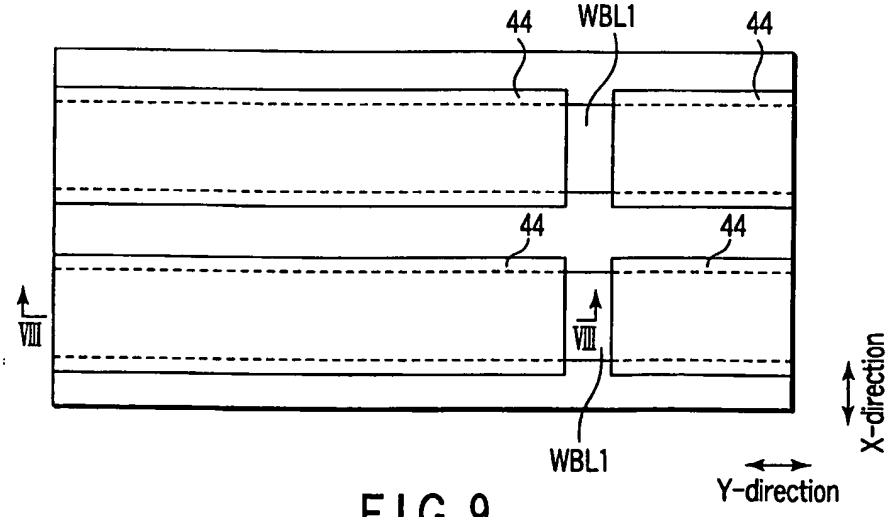
44
WBL1
44
44
44
VIII
VIII
WBL1
X-direction
Y-direction

FIG. 9

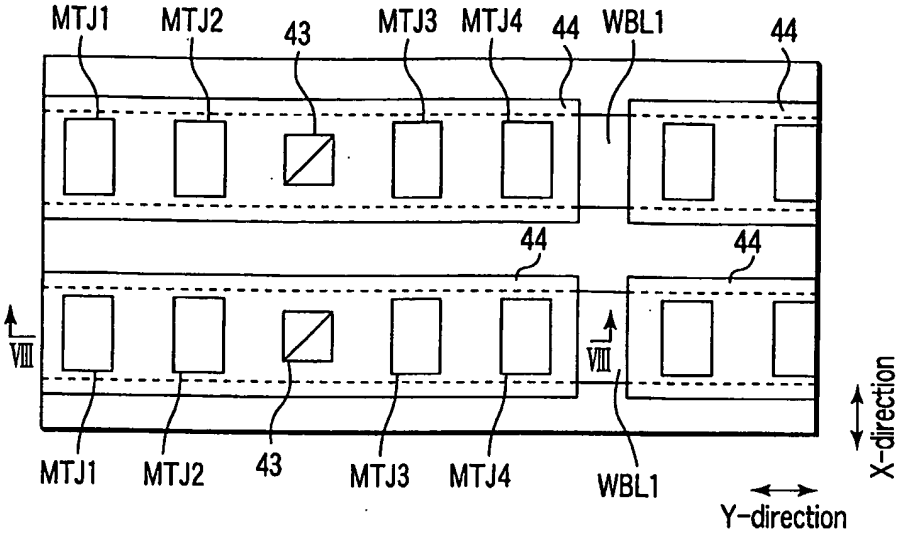
MTJ1
MTJ2
43
MTJ3
MTJ4
44
WBL1
44
44
44
VIII
VIII
MTJ1
MTJ2
43
MTJ3
MTJ4
WBL1
Y-direction
X-direction

FIG. 10

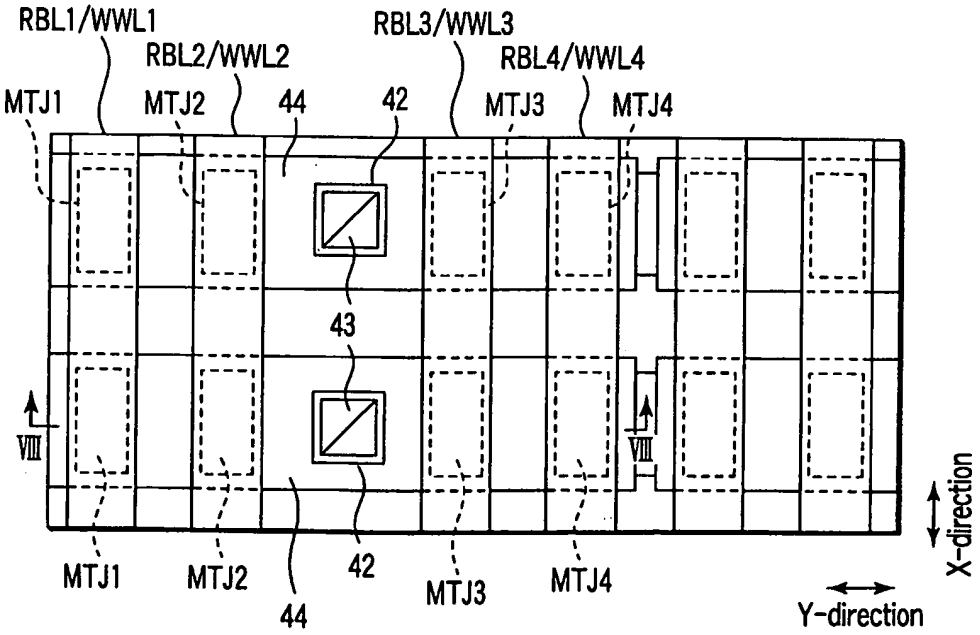
RBL1/WWL1
RBL2/WWL2
RBL3/WWL3
RBL4/WWL4
MTJ1
MTJ2
44
42
MTJ3
MTJ4
43
VIII
VIII
MTJ1
MTJ2
44
42
MTJ3
MTJ4
Y-direction
X-direction

FIG. 11

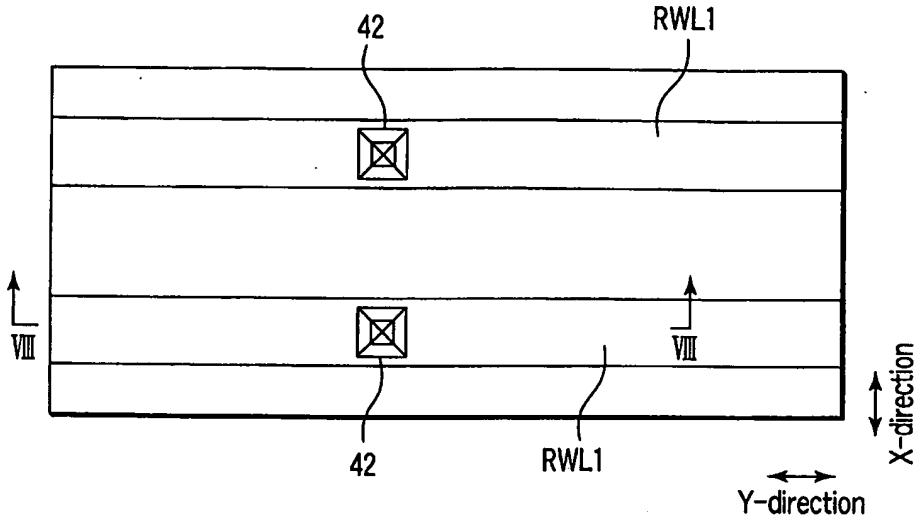
42
RWL1
VIII
VIII
42
RWL1
X-direction
Y-direction

FIG. 12

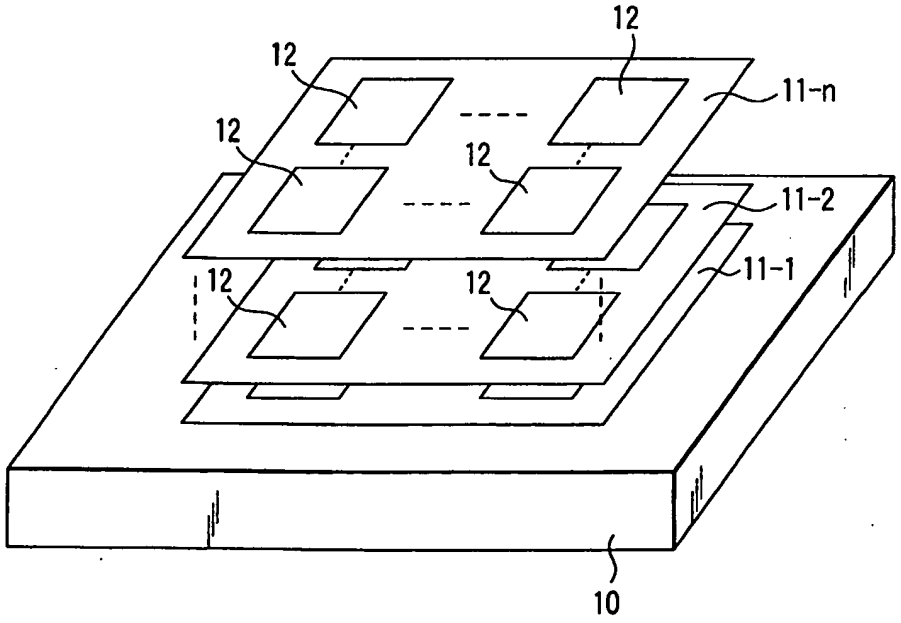
12
12
11-n
12
12
11-2
11-1
12
12
10

FIG. 13

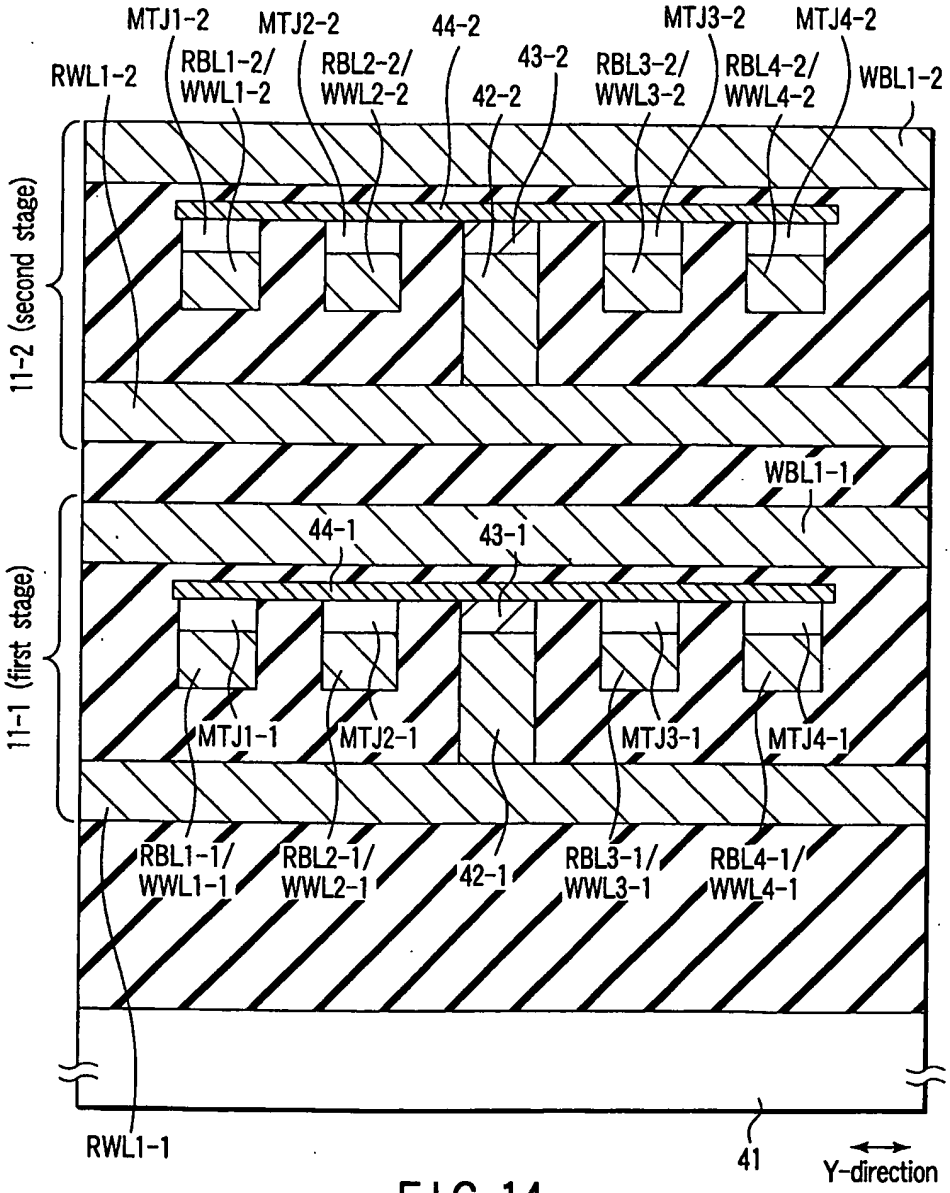
MTJ1-2
MTJ2-2
44-2
MTJ3-2
MTJ4-2
RWL1-2
RBL1-2/
WWL1-2
RBL2-2/
WWL2-2
42-2
43-2
RBL3-2/
WWL3-2
RBL4-2/
WWL4-2
WBL1-2
11-2 (second stage)
WBL1-1
44-1
43-1
11-1 (first stage)
MTJ1-1
MTJ2-1
MTJ3-1
MTJ4-1
RBL1-1/
WWL1-1
RBL2-1/
WWL2-1
42-1
RBL3-1/
WWL3-1
RBL4-1/
WWL4-1
RWL1-1
41
Y-direction

FIG. 14

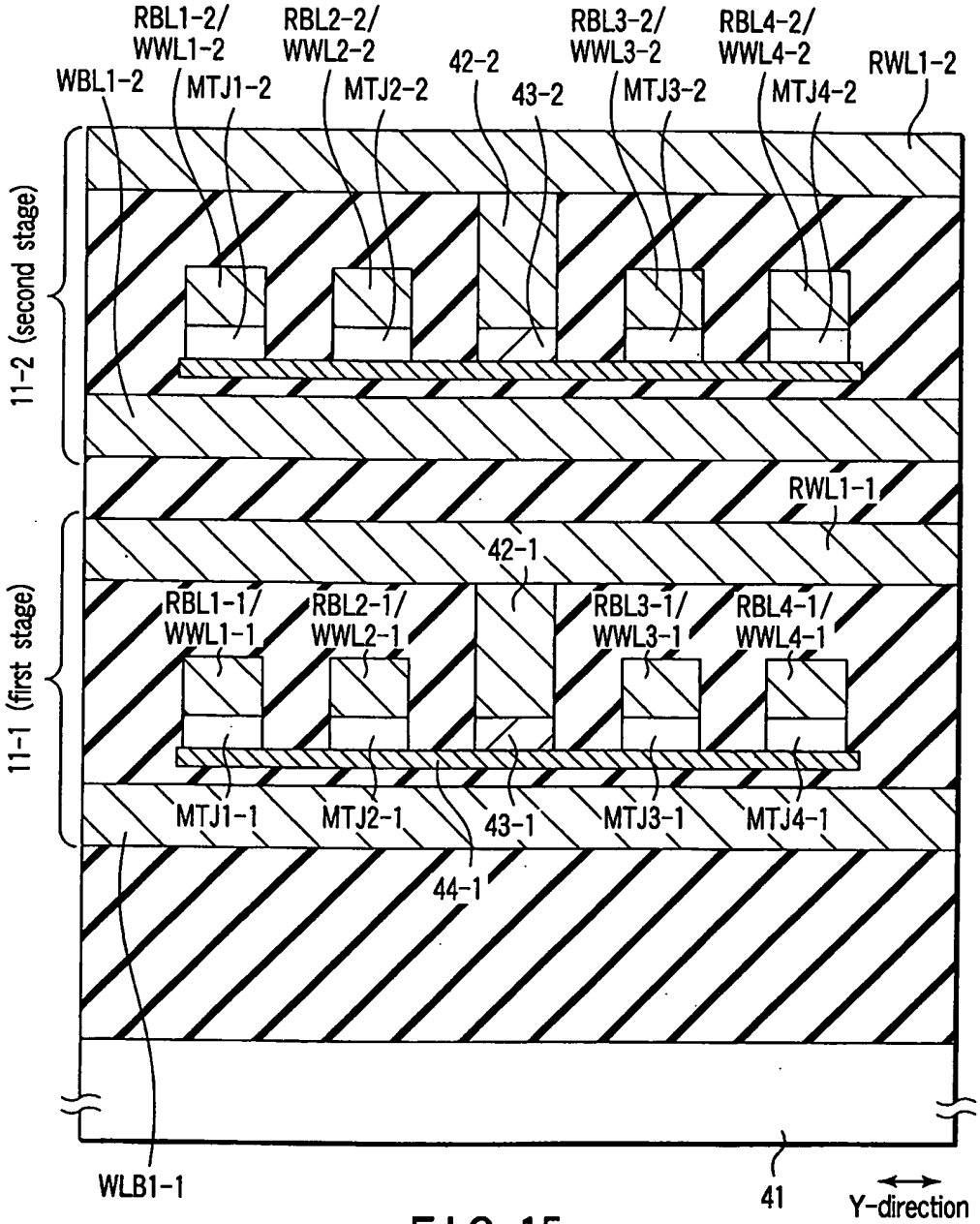
RBL1-2/
WWL1-2
RBL2-2/
WWL2-2
RBL3-2/
WWL3-2
RBL4-2/
WWL4-2
RWL1-2
WBL1-2
MTJ1-2
MTJ2-2
42-2
43-2
MTJ3-2
MTJ4-2
11-2 (second stage)
RWL1-1
42-1
RBL1-1/
WWL1-1
RBL2-1/
WWL2-1
RBL3-1/
WWL3-1
RBL4-1/
WWL4-1
11-1 (first stage)
MTJ1-1
MTJ2-1
43-1
MTJ3-1
MTJ4-1
44-1
WLB1-1
41
Y-direction

FIG. 15

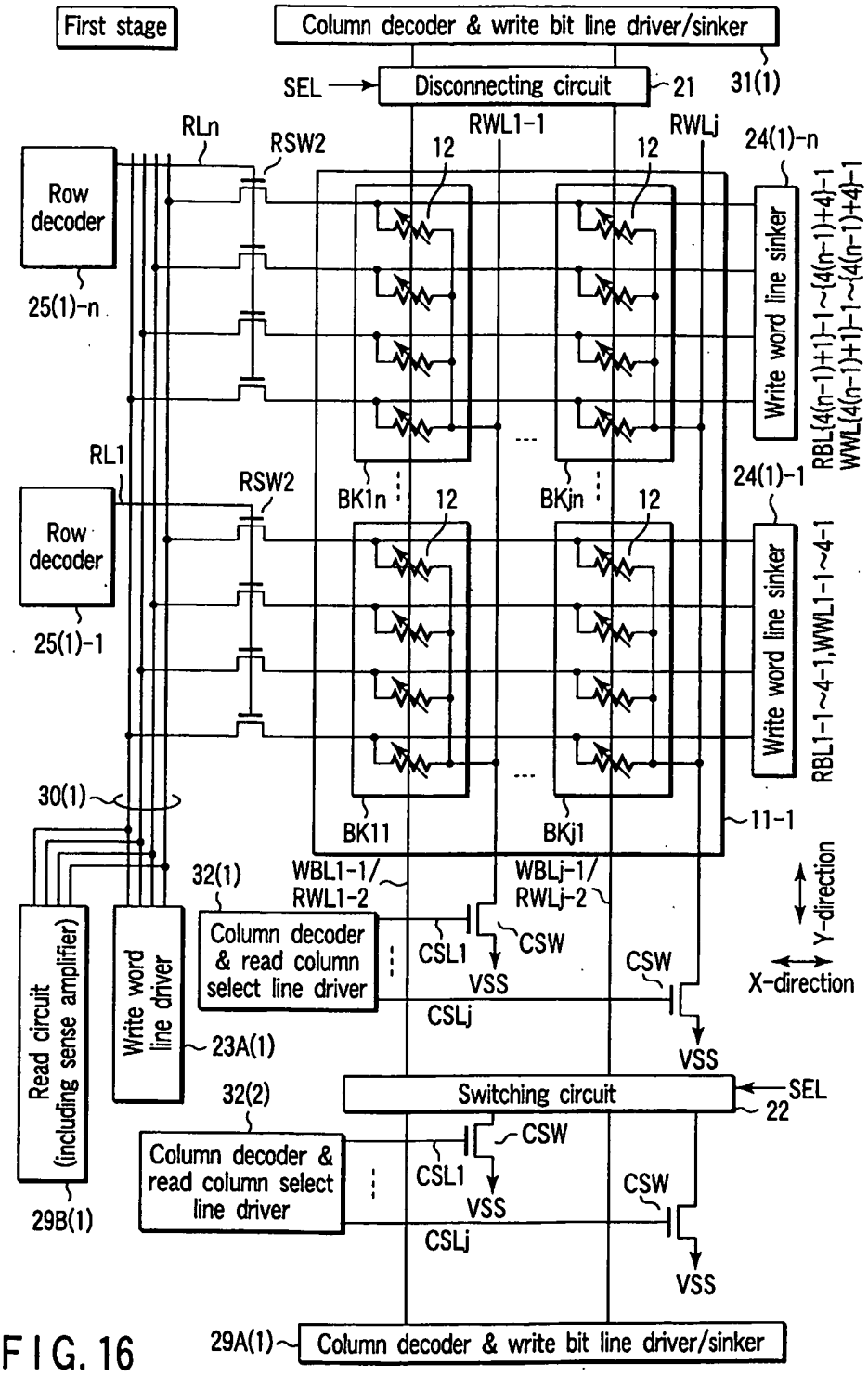
First stage
Column decoder & write bit line driver/sinker
SEL
Disconnecting circuit
21
31(1)
RLn
RSW2
RWL1-1
RWLj
12
24(1)-n
Row decoder
25(1)-n
Write word line sinker
RBL{4(n-1)+1}-1~{4(n-1)+4}-1
WWL{4(n-1)+1}-1~{4(n-1)+4}-1
RL1
RSW2
BK1n
BKjn
24(1)-1
Row decoder
25(1)-1
RBL1-1~4-1,WWL1-1~4-1
30(1)
BK11
BKj1
11-1
32(1)
WBL1-1/RWL1-2
WBLj-1/RWLj-2
Y-direction
X-direction
Column decoder & read column select line driver
CSL1
CSW
VSS
CSLj
Read circuit (including sense amplifier)
Write word line driver
23A(1)
32(2)
Switching circuit
SEL
22
29B(1)
29A(1)

FIG. 16

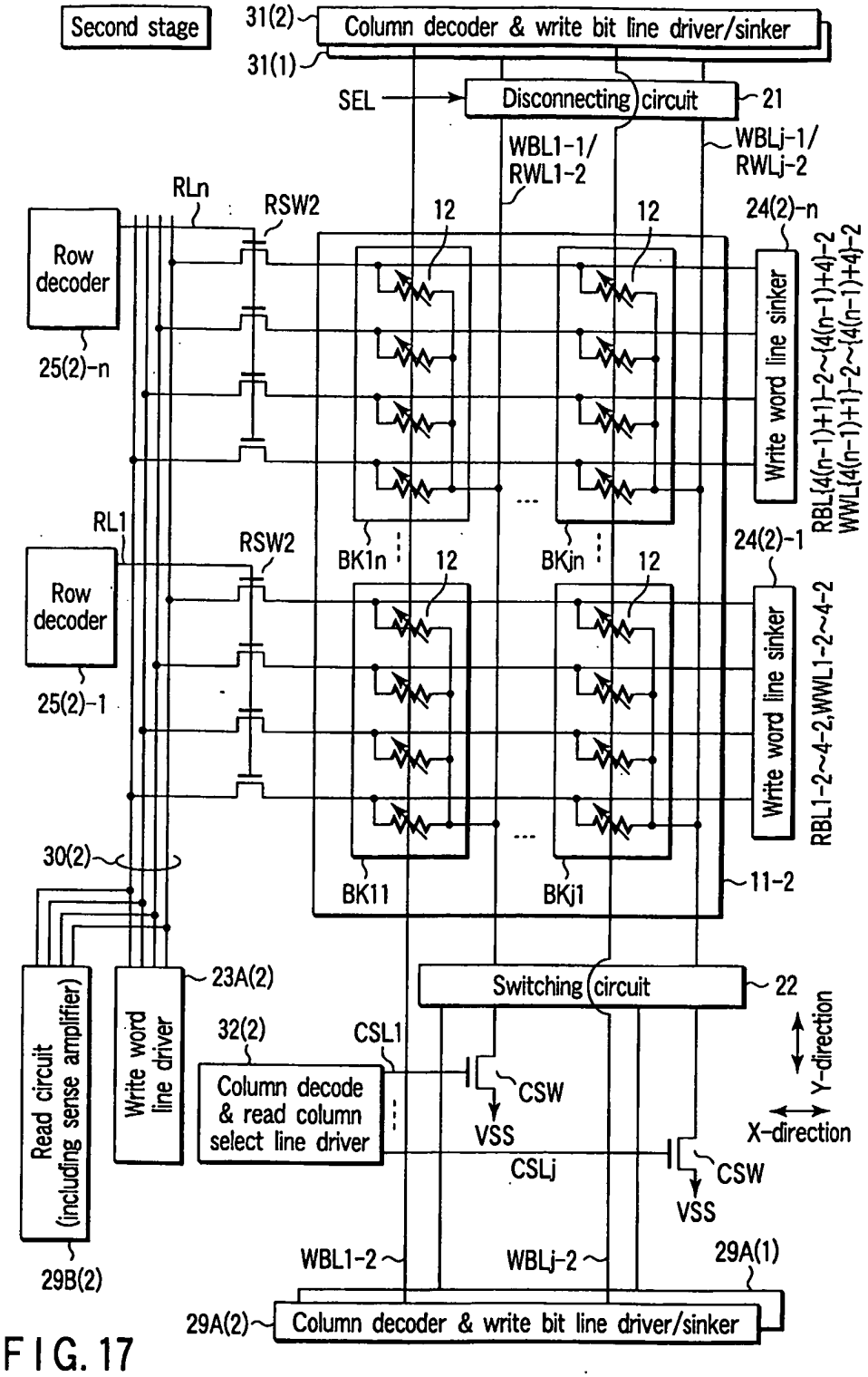
Second stage
31(2)
Column decoder & write bit line driver/sinker
31(1)
SEL
Disconnecting circuit
21
WBL1-1/
RWL1-2
WBLj-1/
RWLj-2
RLn
RSW2
12
12
24(2)-n
Row decoder
25(2)-n
Write word line sinker
RBL{4(n-1)+1}-2~{4(n-1)+4}-2
WWL{4(n-1)+1}-2~{4(n-1)+4}-2
RL1
RSW2
BK1n
12
BKjn
12
24(2)-1
Row decoder
25(2)-1
Write word line sinker
RBL1-2~4-2,WWL1-2~4-2
30(2)
BK11
BKj1
11-2
Switching circuit
22
23A(2)
32(2)
CSL1
Read circuit (including sense amplifier)
Write word line driver
Column decode & read column select line driver
CSW
VSS
CSLj
CSW
VSS
Y-direction
X-direction
29B(2)
WBL1-2
WBLj-2
29A(1)
29A(2)
Column decoder & write bit line driver/sinker

FIG. 17

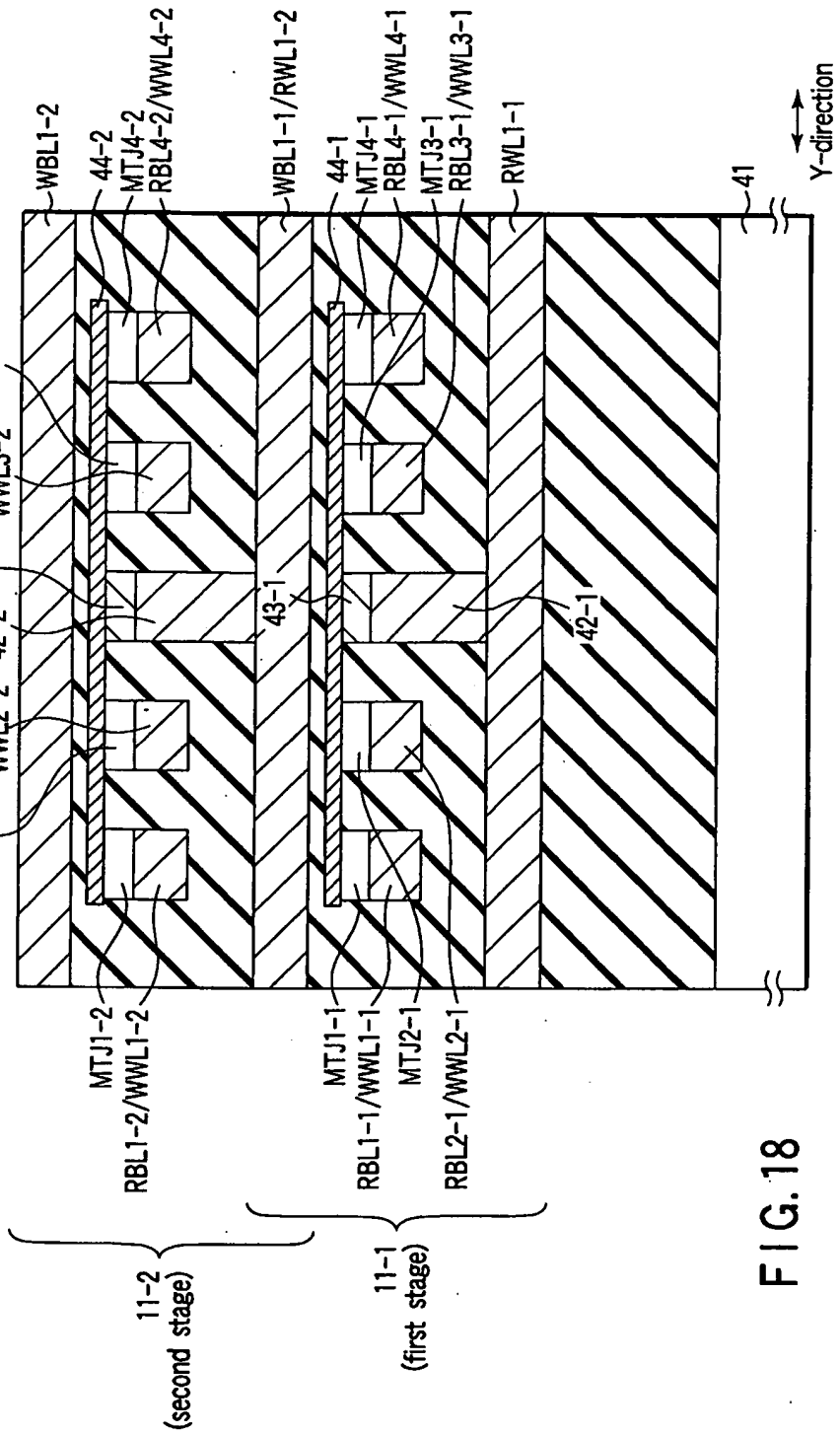
WBL1-2
44-2
MTJ4-2
RBL4-2/WWL4-2
WBL1-1/RWL1-2
44-1
MTJ4-1
RBL4-1/WWL4-1
MTJ3-1
RBL3-1/WWL3-1
RWL1-1
41
Y-direction
MTJ3-2
RBL3-2/
WWL3-2
43-2
42-2
RBL2-2/
WWL2-2
MTJ2-2
43-1
42-1
MTJ1-2
RBL1-2/WWL1-2
MTJ1-1
RBL1-1/WWL1-1
MTJ2-1
RBL2-1/WWL2-1
11-2
(second stage)
11-1
(first stage)

FIG. 18

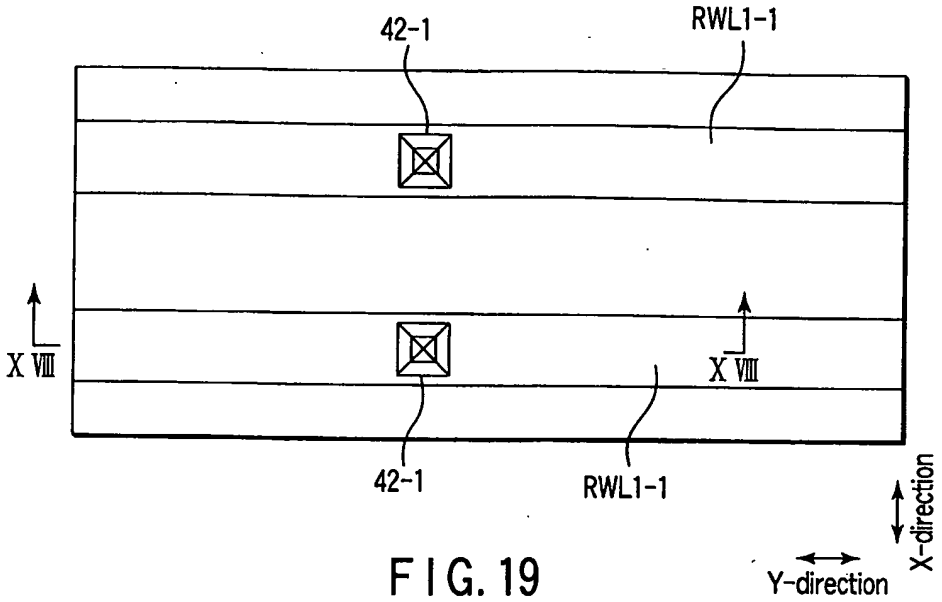
42-1
RWL1-1
X VIII
X VIII
42-1
RWL1-1
X-direction
Y-direction

FIG. 19

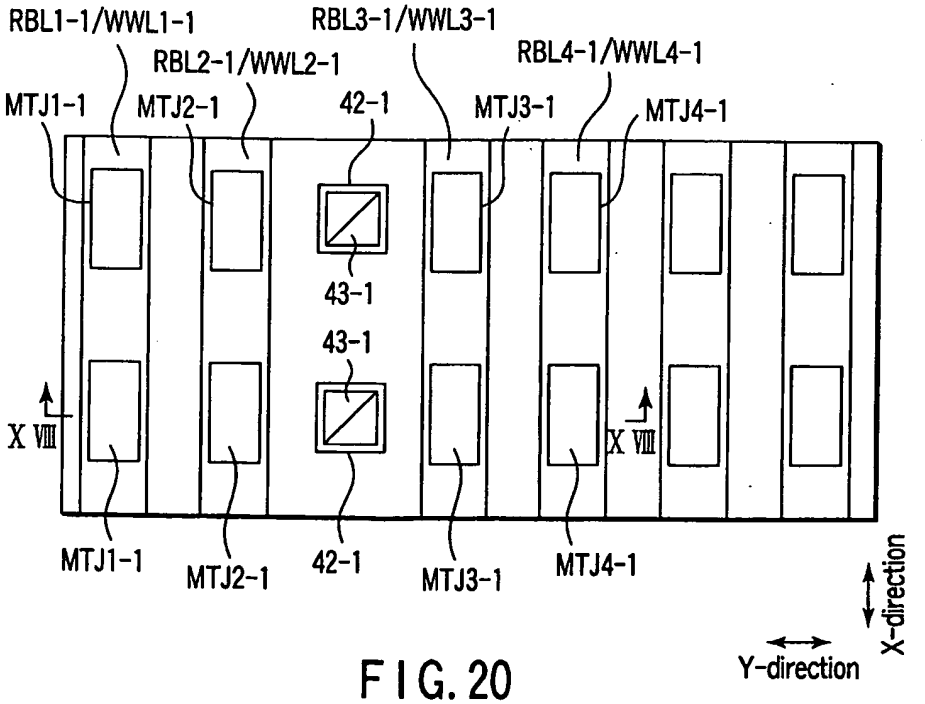
RBL1-1/WWL1-1
RBL2-1/WWL2-1
RBL3-1/WWL3-1
RBL4-1/WWL4-1
MTJ1-1
MTJ2-1
42-1
MTJ3-1
MTJ4-1
43-1
43-1
X VIII
X VIII
MTJ1-1
MTJ2-1
42-1
MTJ3-1
MTJ4-1
X-direction
Y-direction

FIG. 20

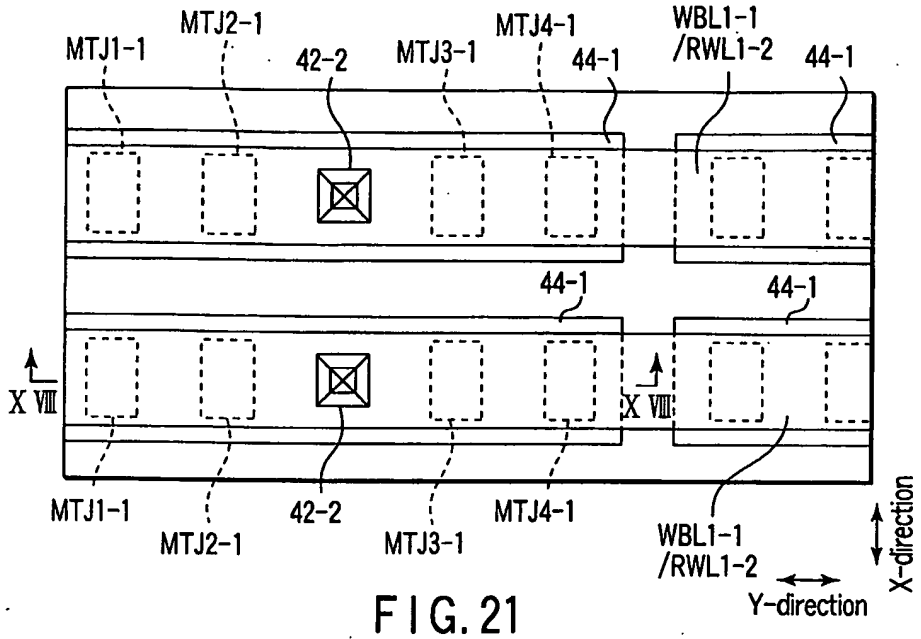
MTJ1-1
MTJ2-1
42-2
MTJ3-1
MTJ4-1
44-1
WBL1-1
/RWL1-2
44-1
44-1
44-1
X VIII
X VIII
MTJ1-1
MTJ2-1
42-2
MTJ3-1
MTJ4-1
WBL1-1
/RWL1-2
X-direction
Y-direction

FIG. 21

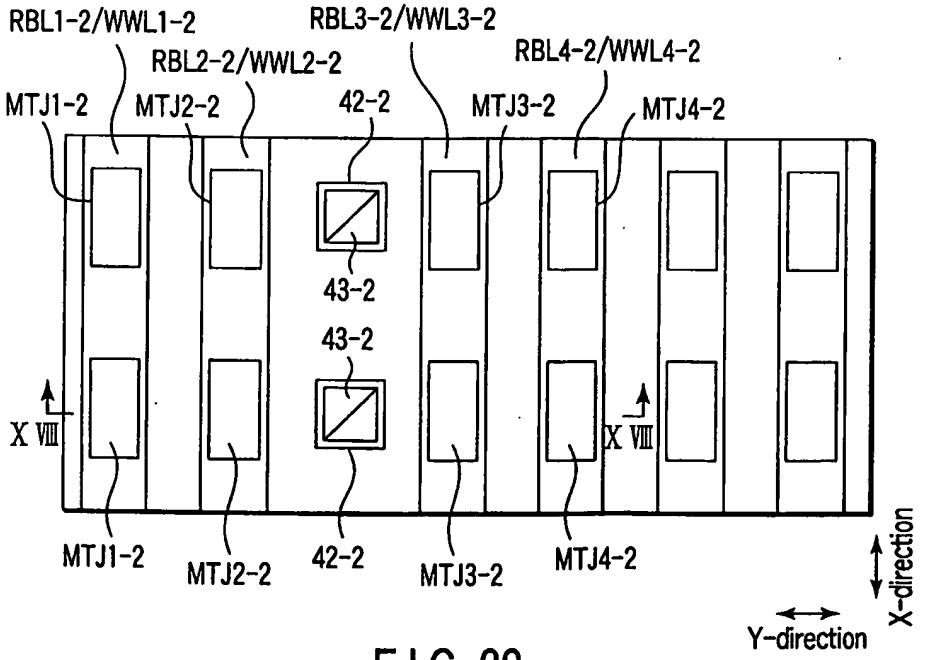
RBL1-2/WWL1-2
RBL2-2/WWL2-2
RBL3-2/WWL3-2
RBL4-2/WWL4-2
MTJ1-2
MTJ2-2
42-2
MTJ3-2
MTJ4-2
43-2
43-2
X VIII
X VIII
MTJ1-2
MTJ2-2
42-2
MTJ3-2
MTJ4-2
X-direction
Y-direction

FIG. 22

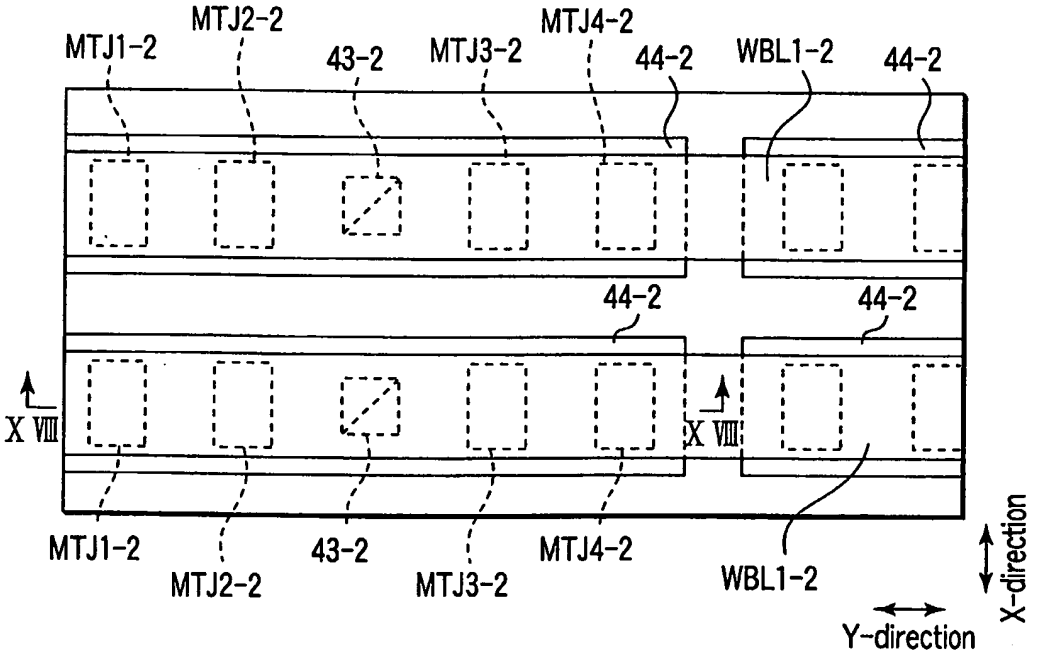
MTJ1-2
MTJ2-2
43-2
MTJ3-2
MTJ4-2
44-2
WBL1-2
44-2
44-2
44-2
X VIII
X VIII
MTJ1-2
MTJ2-2
43-2
MTJ3-2
MTJ4-2
WBL1-2
X-direction
Y-direction

FIG. 23

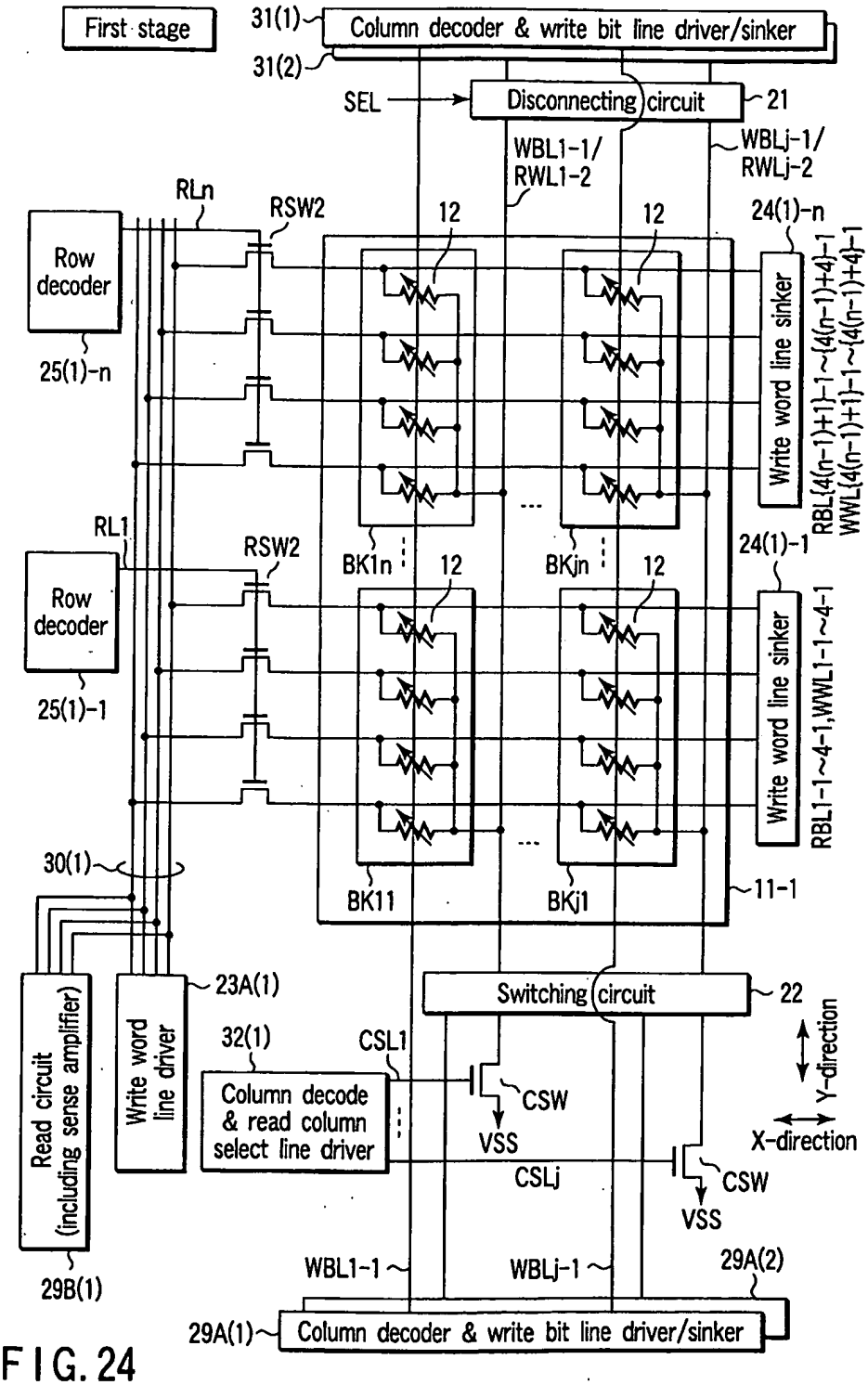
First stage
31(1)
Column decoder & write bit line driver/sinker
31(2)
SEL
Disconnecting circuit
21
WBL1-1/
RWL1-2
WBLj-1/
RWLj-2
RLn
RSW2
12
12
24(1)-n
Row decoder
25(1)-n
Write word line sinker
RBL{4(n-1)+1}-1~{4(n-1)+4}-1
WWL{4(n-1)+1}-1~{4(n-1)+4}-1
RL1
RSW2
BK1n
12
BKjn
12
24(1)-1
Row decoder
25(1)-1
Write word line sinker
RBL1-1~4-1,WWL1-1~4-1
30(1)
BK11
BKj1
11-1
Read circuit (including sense amplifier)
29B(1)
Write word line driver
23A(1)
Switching circuit
22
32(1)
CSL1
Column decode & read column select line driver
CSW
VSS
CSLj
CSW
VSS
Y-direction
X-direction
WBL1-1
WBLj-1
29A(2)
29A(1)
Column decoder & write bit line driver/sinker

FIG. 24

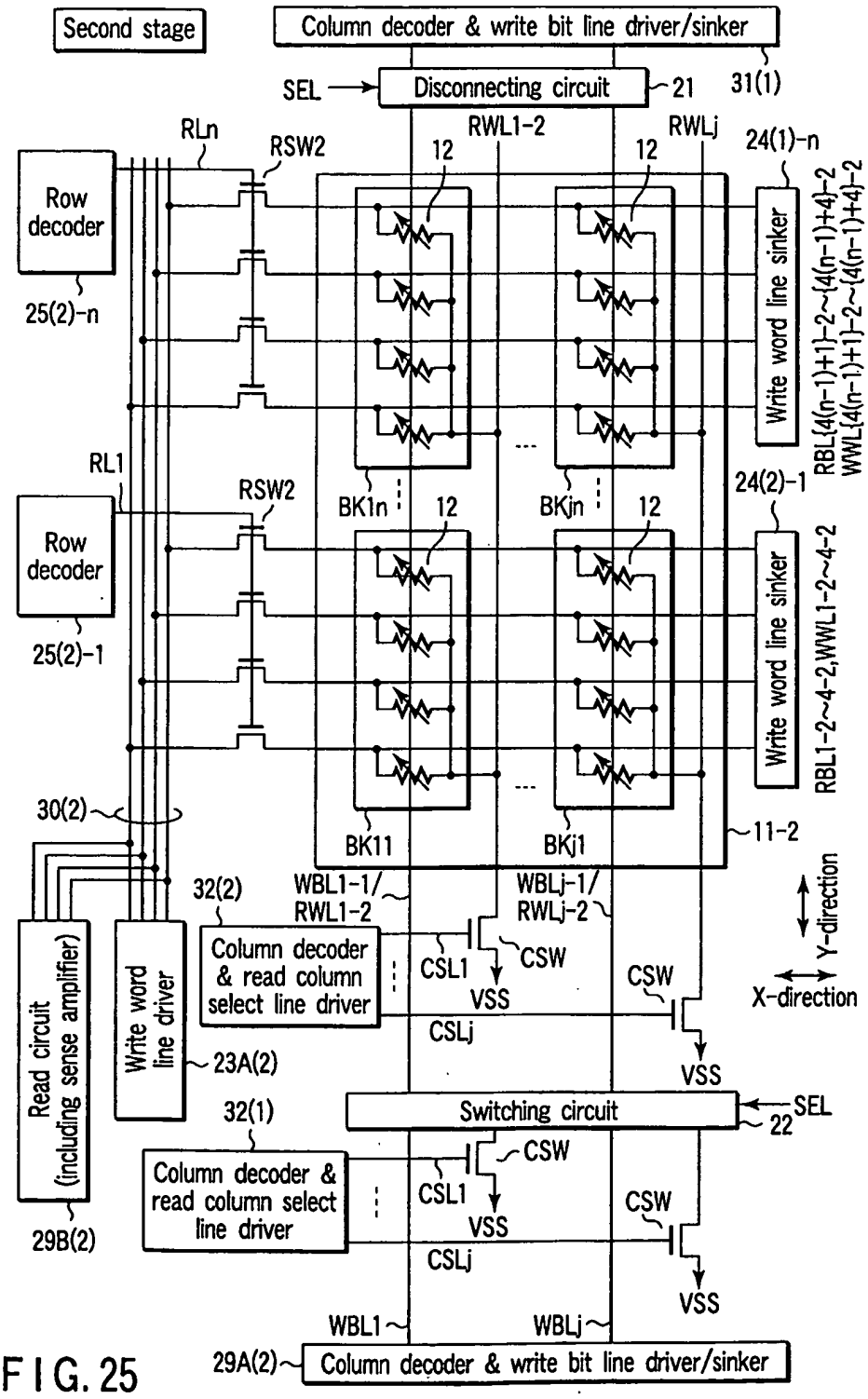
Second stage
Column decoder & write bit line driver/sinker
SEL
Disconnecting circuit
21
31(1)
RLn
RSW2
RWL1-2
RWLj
12
24(1)-n
Row decoder
25(2)-n
Write word line sinker
RBL{4(n-1)+1}-2~{4(n-1)+4}-2
WWL{4(n-1)+1}-2~{4(n-1)+4}-2
RL1
RSW2
BK1n
BKjn
24(2)-1
Row decoder
25(2)-1
RBL1-2~4-2,WWL1-2~4-2
30(2)
BK11
BKj1
11-2
32(2)
WBL1-1/RWL1-2
WBLj-1/RWLj-2
Y-direction
X-direction
Read circuit (including sense amplifier)
Write word line driver
Column decoder & read column select line driver
CSL1
CSW
VSS
CSLj
23A(2)
32(1)
Switching circuit
22
SEL
Column decoder & read column select line driver
29B(2)
WBL1
WBLj
29A(2)
Column decoder & write bit line driver/sinker

FIG. 25

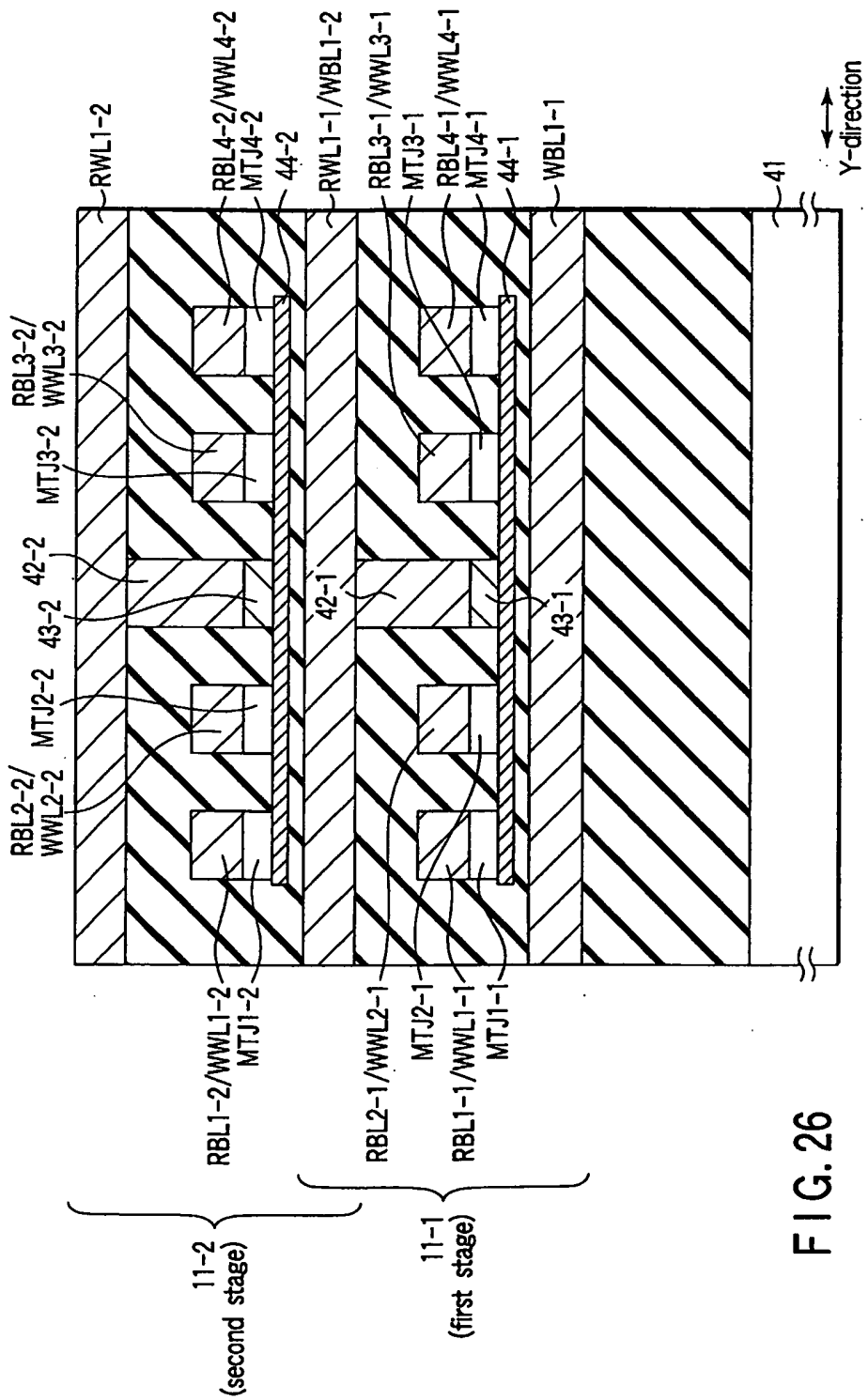
RWL1-2
RBL4-2/WWL4-2
MTJ4-2
44-2
RWL1-1/WBL1-2
RBL3-1/WWL3-1
MTJ3-1
RBL4-1/WWL4-1
MTJ4-1
44-1
WBL1-1
41
Y-direction
RBL3-2/
WWL3-2
MTJ3-2
42-2
43-2
MTJ2-2
RBL2-2/
WWL2-2
42-1
43-1
RBL1-2/WWL1-2
MTJ1-2
RBL2-1/WWL2-1
MTJ2-1
RBL1-1/WWL1-1
MTJ1-1
11-2
(second stage)
11-1
(first stage)

FIG. 26

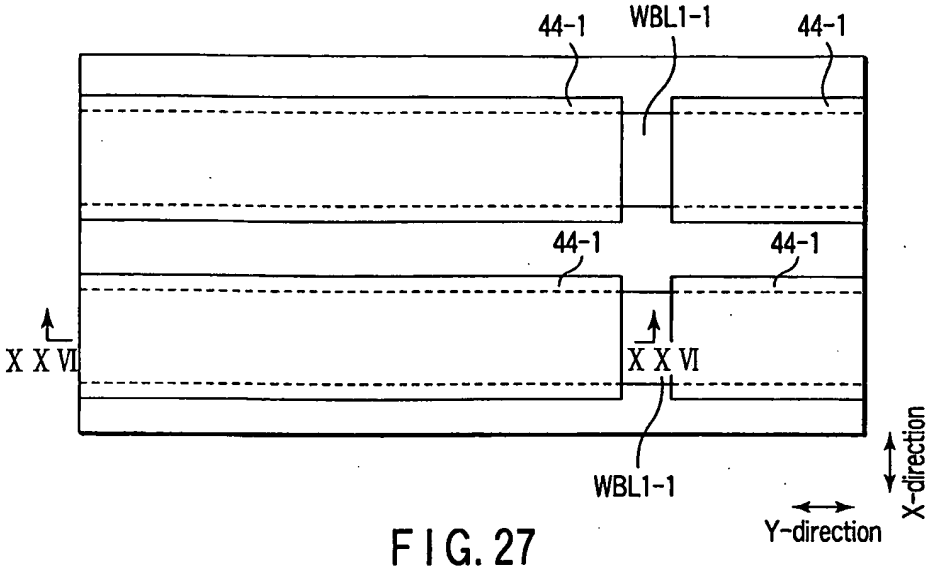
44-1
WBL1-1
44-1
44-1
44-1
X X VI
X X VI
WBL1-1
X-direction
Y-direction

FIG. 27

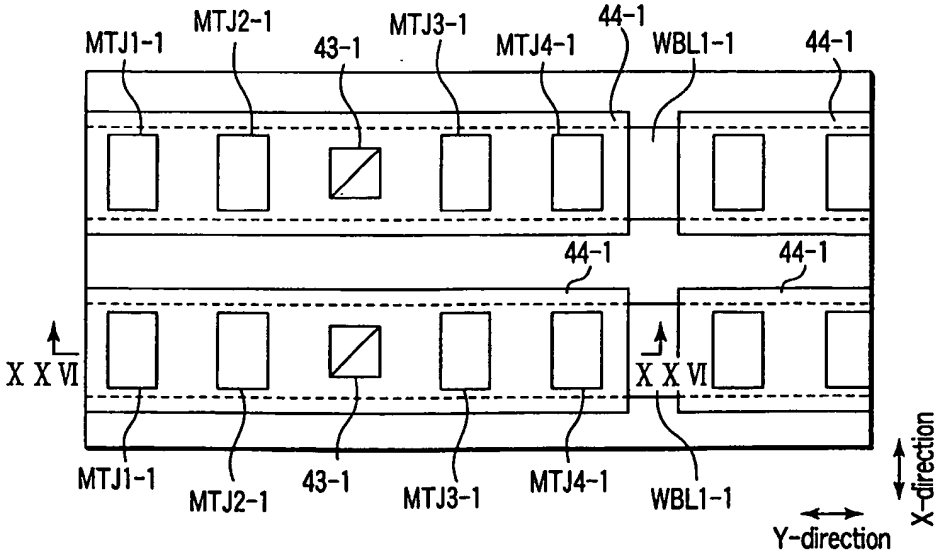
MTJ1-1
MTJ2-1
43-1
MTJ3-1
MTJ4-1
44-1
WBL1-1
44-1
44-1
44-1
X X VI
X X VI
MTJ1-1
MTJ2-1
43-1
MTJ3-1
MTJ4-1
WBL1-1
X-direction
Y-direction

FIG. 28

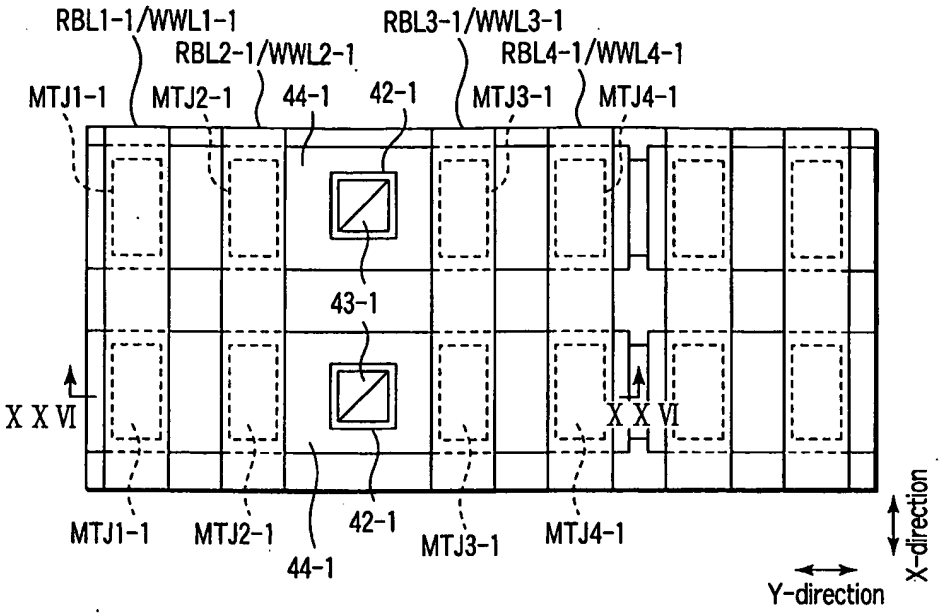
RBL1-1/WWL1-1
RBL2-1/WWL2-1
RBL3-1/WWL3-1
RBL4-1/WWL4-1
MTJ1-1
MTJ2-1
44-1
42-1
MTJ3-1
MTJ4-1
43-1
X X VI
X X VI
MTJ1-1
MTJ2-1
42-1
44-1
MTJ3-1
MTJ4-1
X-direction
Y-direction

FIG. 29

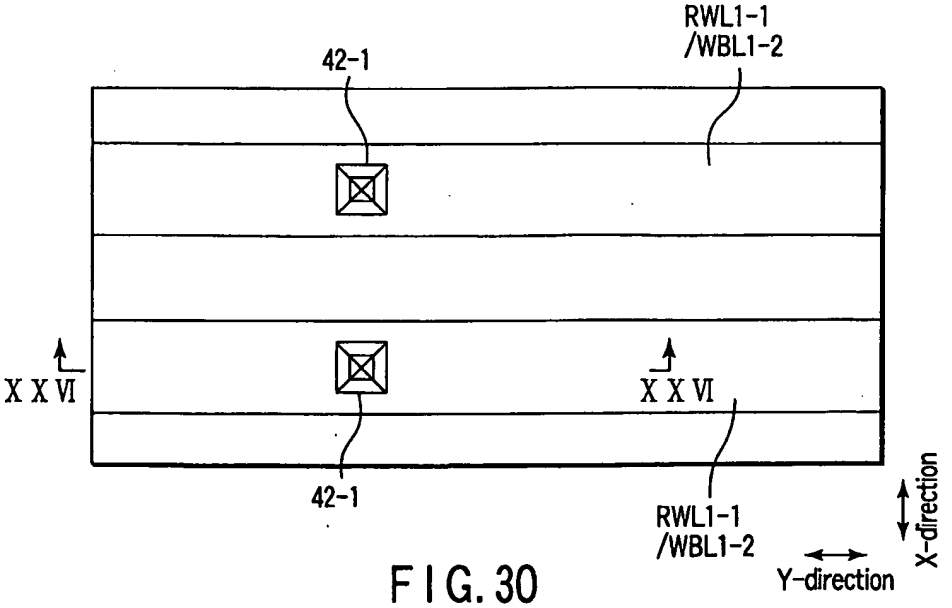
RWL1-1
/WBL1-2
42-1
X X VI
X X VI
42-1
RWL1-1
/WBL1-2
X-direction
Y-direction

FIG. 30

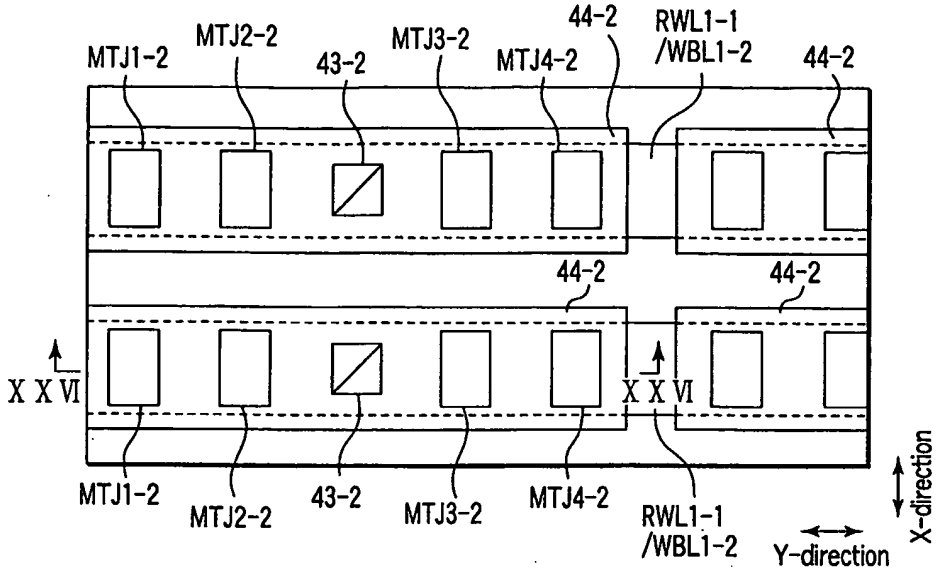
MTJ1-2
MTJ2-2
43-2
MTJ3-2
MTJ4-2
44-2
RWL1-1
/WBL1-2
44-2
44-2
44-2
X X VI
X X VI
MTJ1-2
MTJ2-2
43-2
MTJ3-2
MTJ4-2
RWL1-1
/WBL1-2
Y-direction
X-direction

FIG. 31

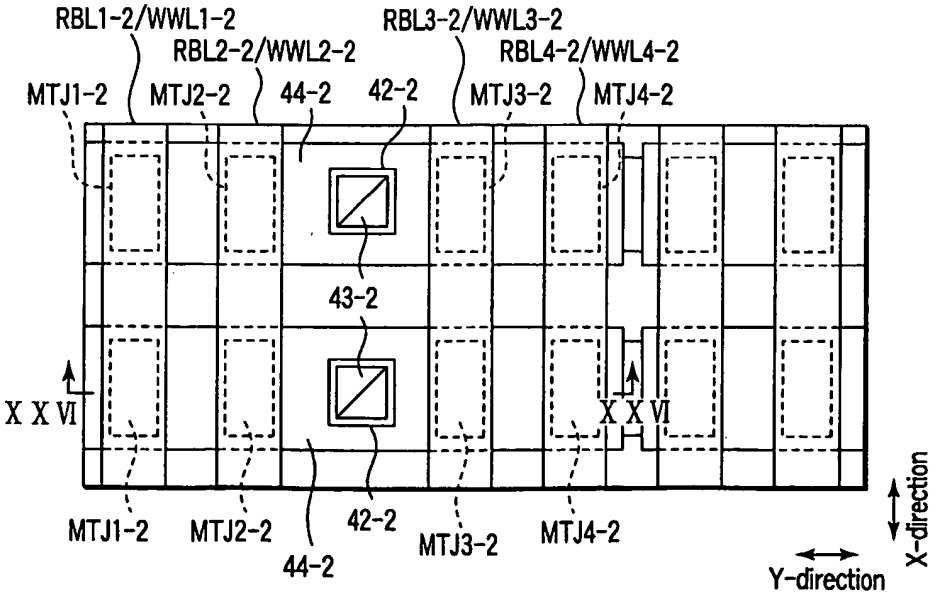
RBL1-2/WWL1-2
RBL2-2/WWL2-2
RBL3-2/WWL3-2
RBL4-2/WWL4-2
MTJ1-2
MTJ2-2
44-2
42-2
MTJ3-2
MTJ4-2
43-2
X X VI
X X VI
MTJ1-2
MTJ2-2
42-2
MTJ3-2
MTJ4-2
44-2
Y-direction
X-direction

FIG. 32

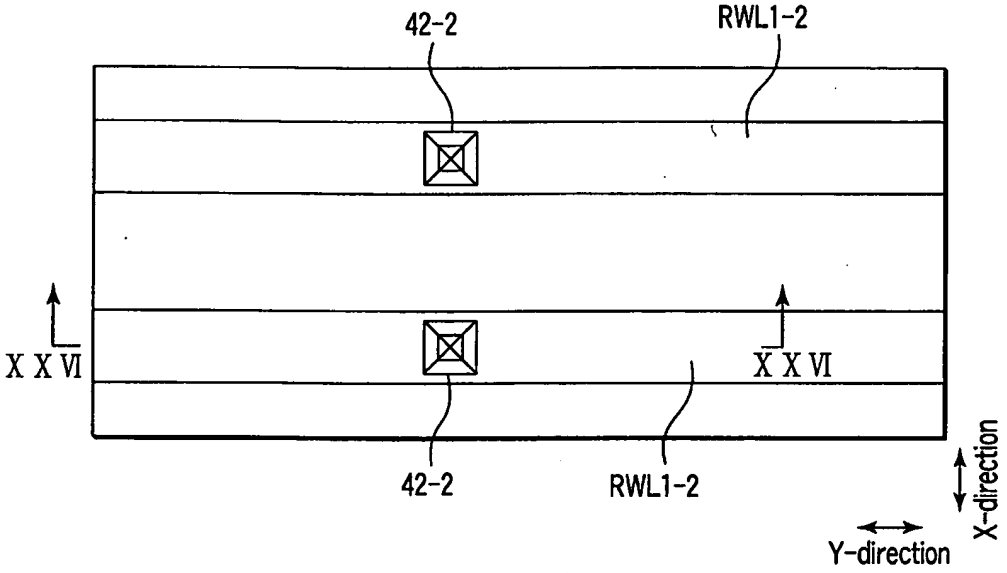

FIG. 33

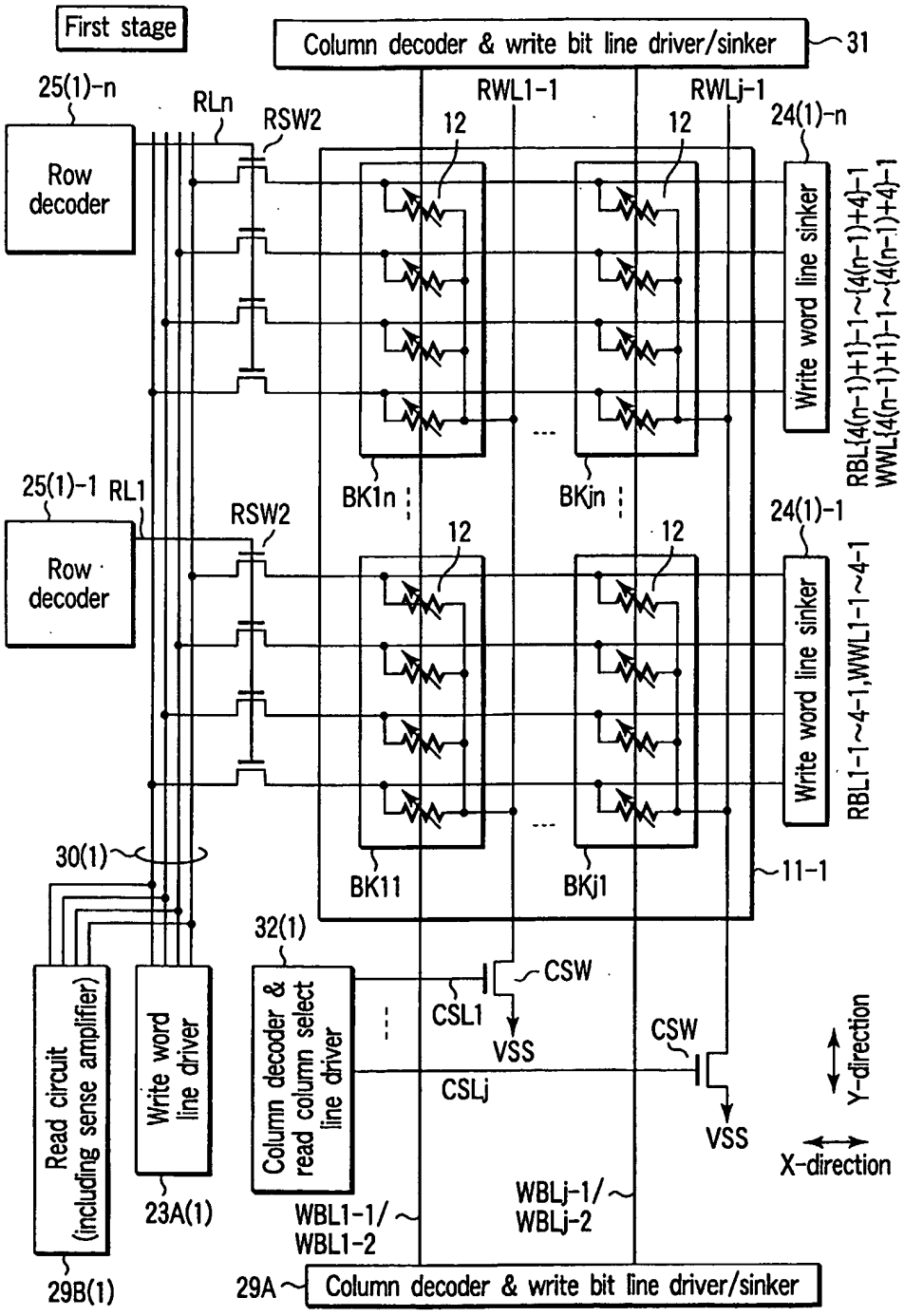
First stage
Column decoder & write bit line driver/sinker
31
25(1)-n
RLn
RSW2
RWL1-1
RWLj-1
12
24(1)-n
Row decoder
Write word line sinker
RBL{4(n-1)+1}-1~{4(n-1)+4}-1
WWL{4(n-1)+1}-1~{4(n-1)+4}-1
25(1)-1
RL1
BK1n
BKjn
Row decoder
24(1)-1
RBL1-1~4-1,WWL1-1~4-1
30(1)
BK11
BKj1
11-1
32(1)
CSW
CSL1
VSS
CSLj
Y-direction
X-direction
Read circuit (including sense amplifier)
Write word line driver
Column decoder & read column select line driver
23A(1)
WBL1-1/ WBL1-2
WBLj-1/ WBLj-2
29B(1)
29A
Column decoder & write bit line driver/sinker

FIG. 34

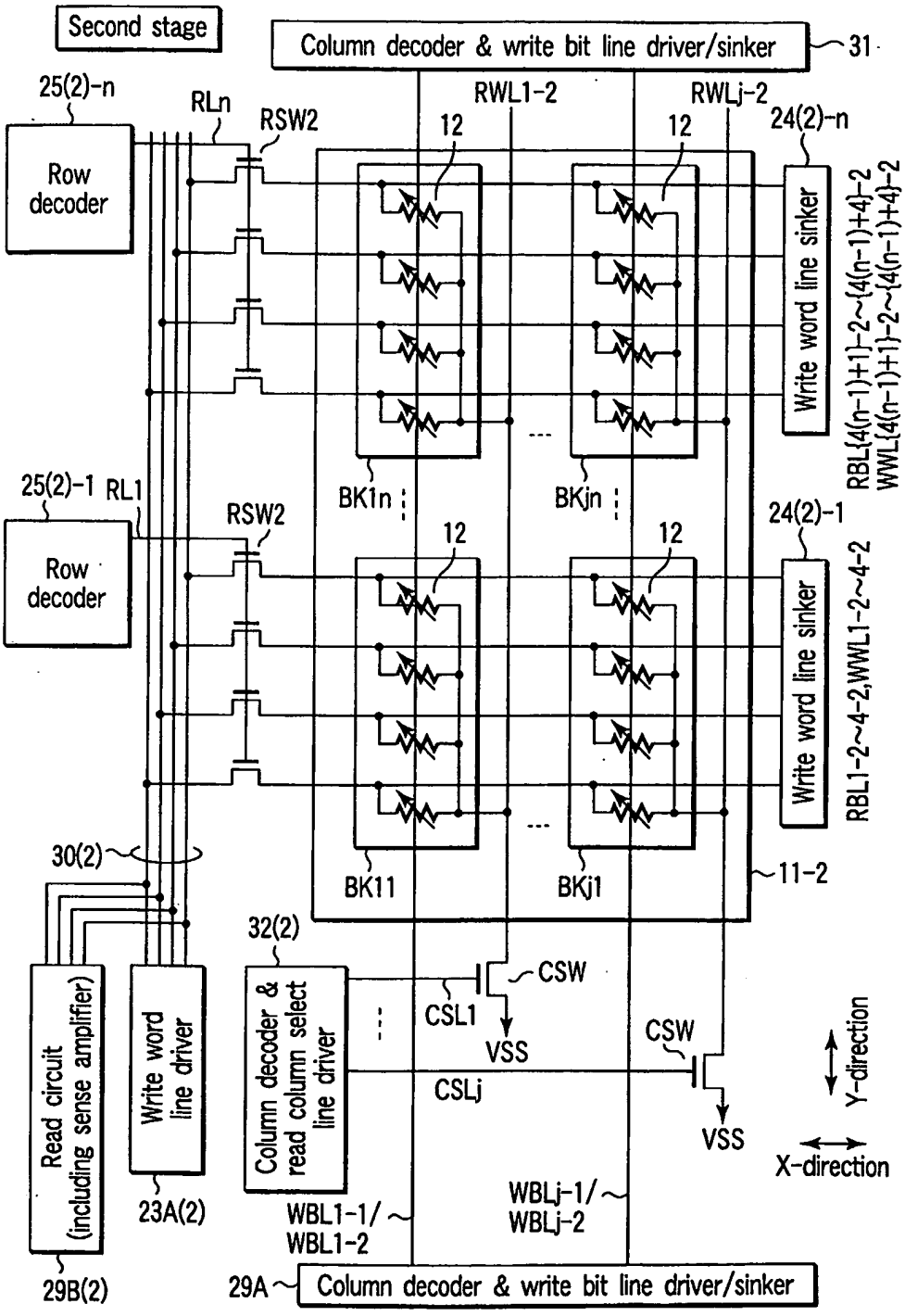
Second stage
Column decoder & write bit line driver/sinker
31
25(2)-n
RLn
RSW2
RWL1-2
RWLj-2
12
24(2)-n
Row decoder
Write word line sinker
RBL{4(n-1)+1}-2~{4(n-1)+4}-2
WWL{4(n-1)+1}-2~{4(n-1)+4}-2
25(2)-1
RL1
BK1n
BKjn
24(2)-1
RBL1-2~4-2,WWL1-2~4-2
30(2)
BK11
BKj1
11-2
32(2)
CSW
CSL1
VSS
CSLj
Y-direction
X-direction
Read circuit (including sense amplifier)
Write word line driver
Column decoder & read column select line driver
23A(2)
WBL1-1/ WBL1-2
WBLj-1/ WBLj-2
29B(2)
29A
Column decoder & write bit line driver/sinker

FIG. 35

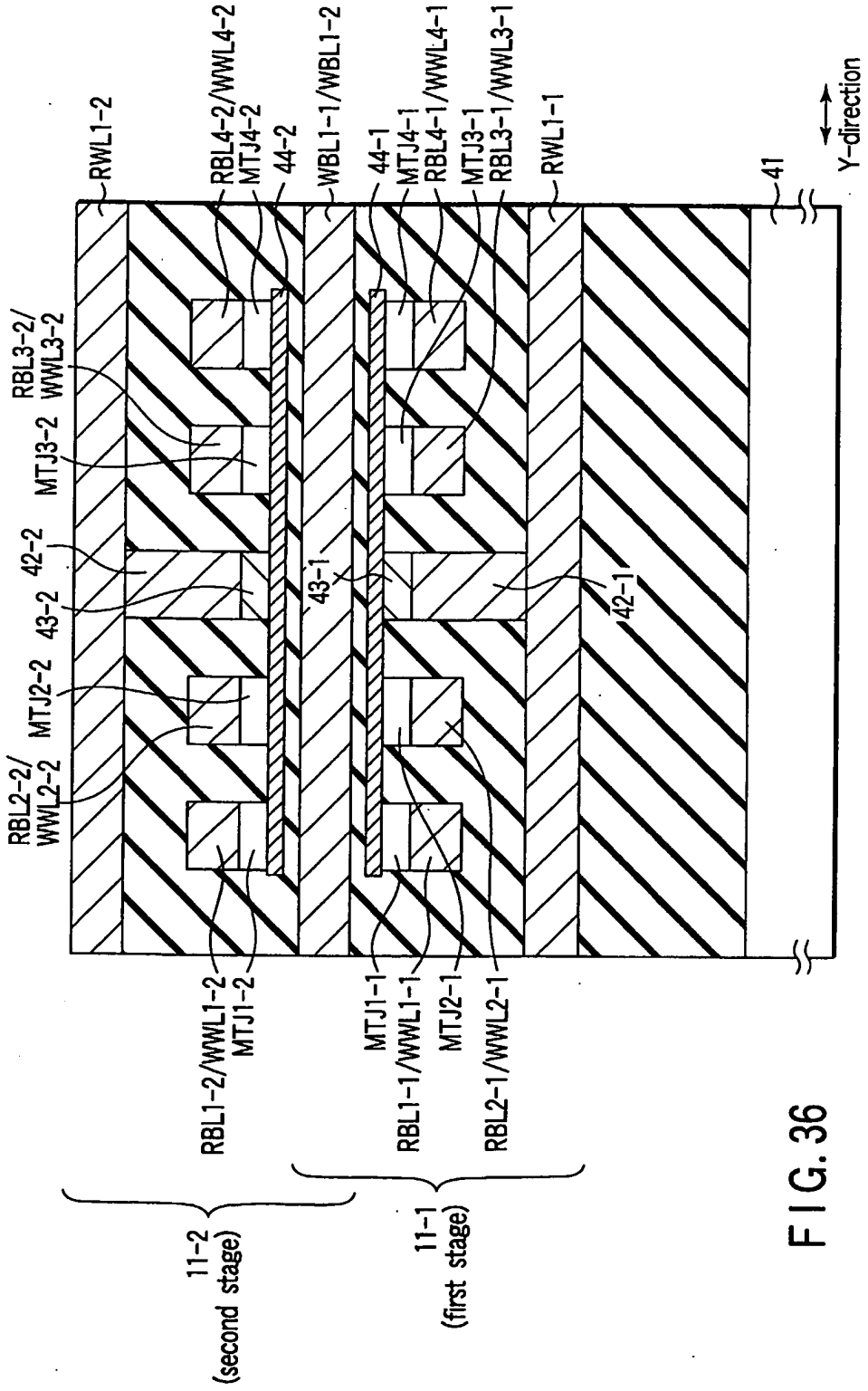
RWL1-2
RBL4-2/WWL4-2
MTJ4-2
44-2
WBL1-1/WBL1-2
44-1
MTJ4-1
RBL4-1/WWL4-1
MTJ3-1
RBL3-1/WWL3-1
RWL1-1
41
Y-direction
RBL3-2/
WWL3-2
MTJ3-2
42-2
43-2
MTJ2-2
RBL2-2/
WWL2-2
43-1
42-1
RBL1-2/WWL1-2
MTJ1-2
MTJ1-1
RBL1-1/WWL1-1
MTJ2-1
RBL2-1/WWL2-1
11-2
(second stage)
11-1
(first stage)

FIG. 36

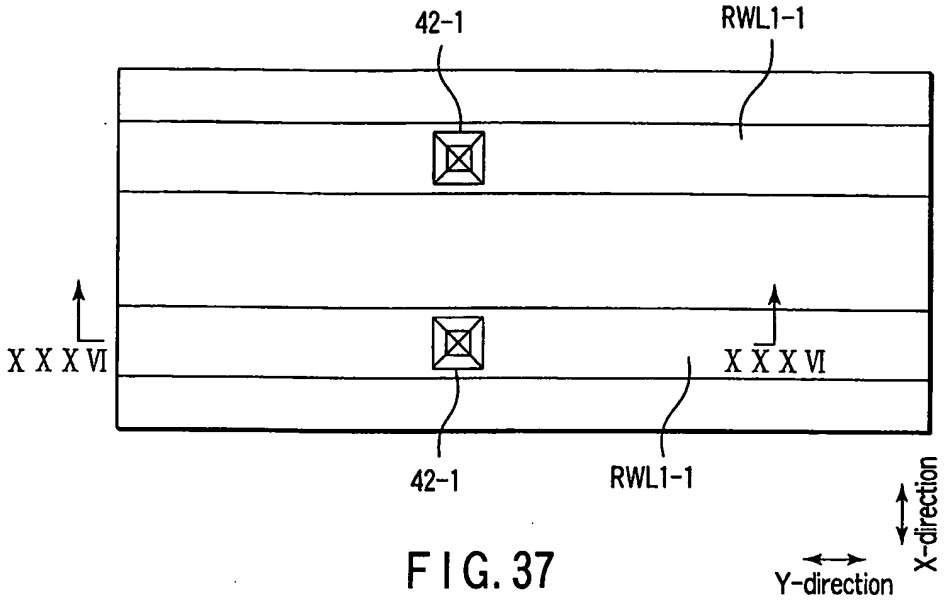
42-1
RWL1-1
X X X VI
X X X VI
42-1
RWL1-1
X-direction
Y-direction

FIG. 37

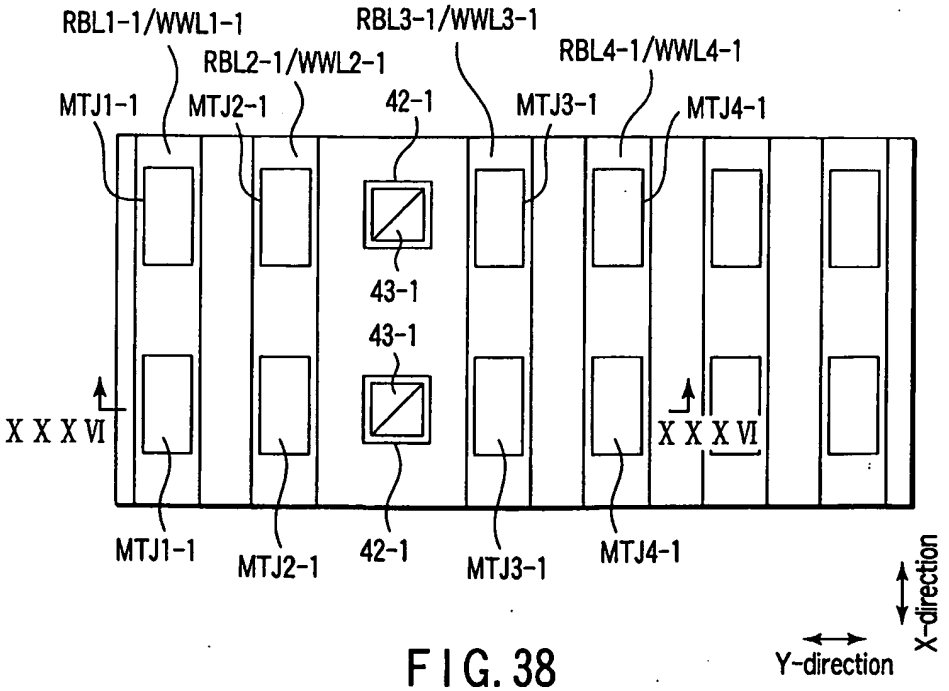
RBL1-1/WWL1-1
RBL2-1/WWL2-1
RBL3-1/WWL3-1
RBL4-1/WWL4-1
MTJ1-1
MTJ2-1
42-1
MTJ3-1
MTJ4-1
43-1
43-1
X X X VI
X X X VI
MTJ1-1
MTJ2-1
42-1
MTJ3-1
MTJ4-1
X-direction
Y-direction

FIG. 38

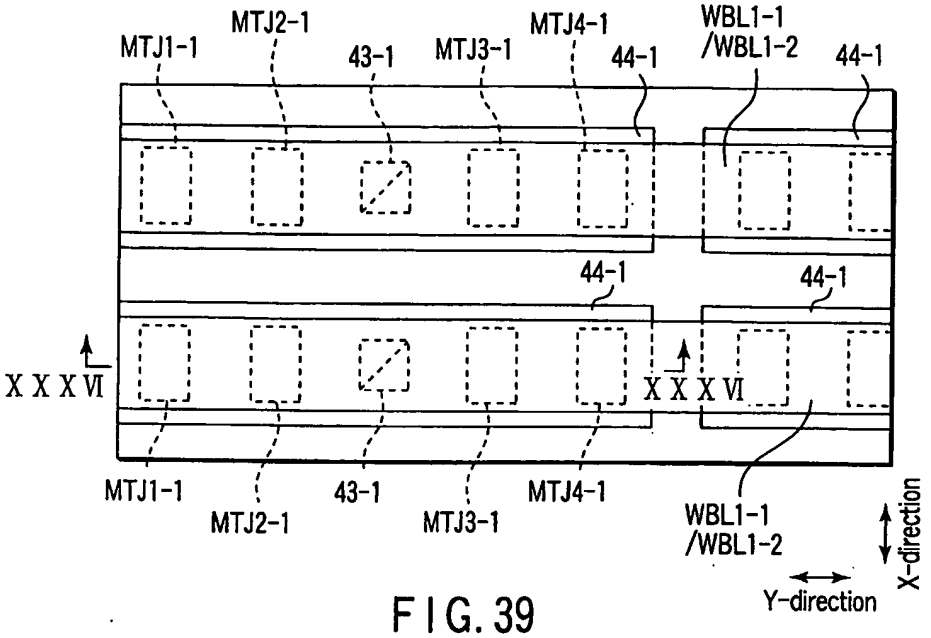
MTJ1-1
MTJ2-1
43-1
MTJ3-1
MTJ4-1
44-1
WBL1-1
/WBL1-2
44-1
44-1
44-1
X X X VI
X X X VI
MTJ1-1
MTJ2-1
43-1
MTJ3-1
MTJ4-1
WBL1-1
/WBL1-2
X-direction
Y-direction

FIG. 39

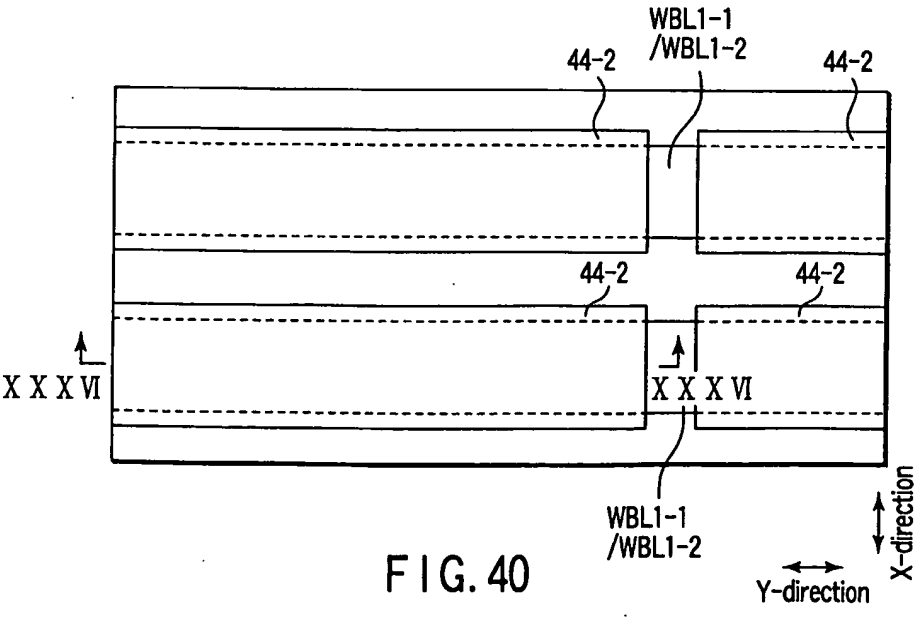
WBL1-1
/WBL1-2
44-2
44-2
44-2
44-2
X X X VI
X X X VI
WBL1-1
/WBL1-2
X-direction
Y-direction

FIG. 40

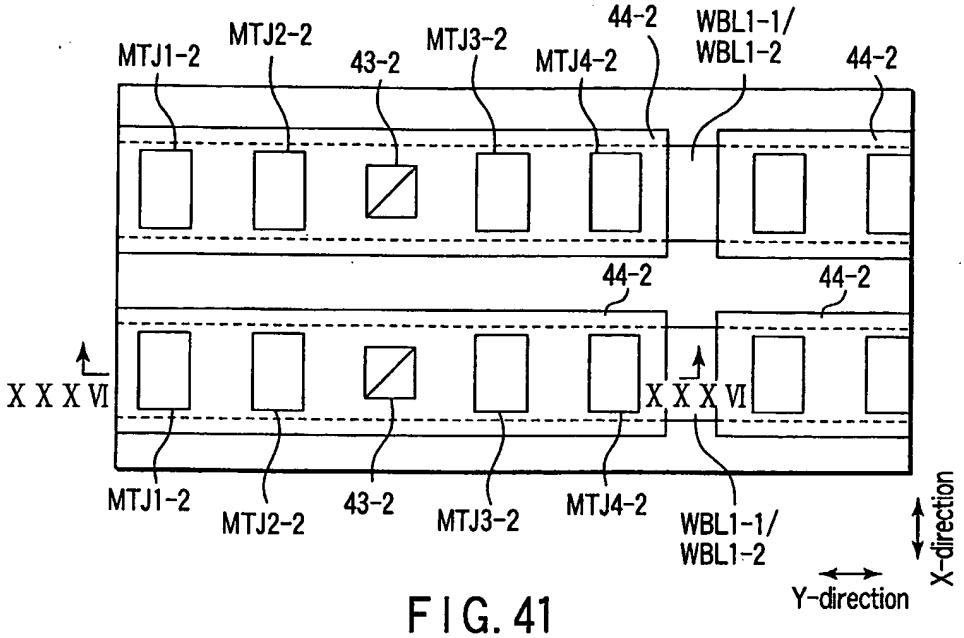
MTJ1-2
MTJ2-2
43-2
MTJ3-2
MTJ4-2
44-2
WBL1-1/
WBL1-2
44-2
44-2
44-2
X X X VI
X X X VI
MTJ1-2
MTJ2-2
43-2
MTJ3-2
MTJ4-2
WBL1-1/
WBL1-2
X-direction
Y-direction

FIG. 41

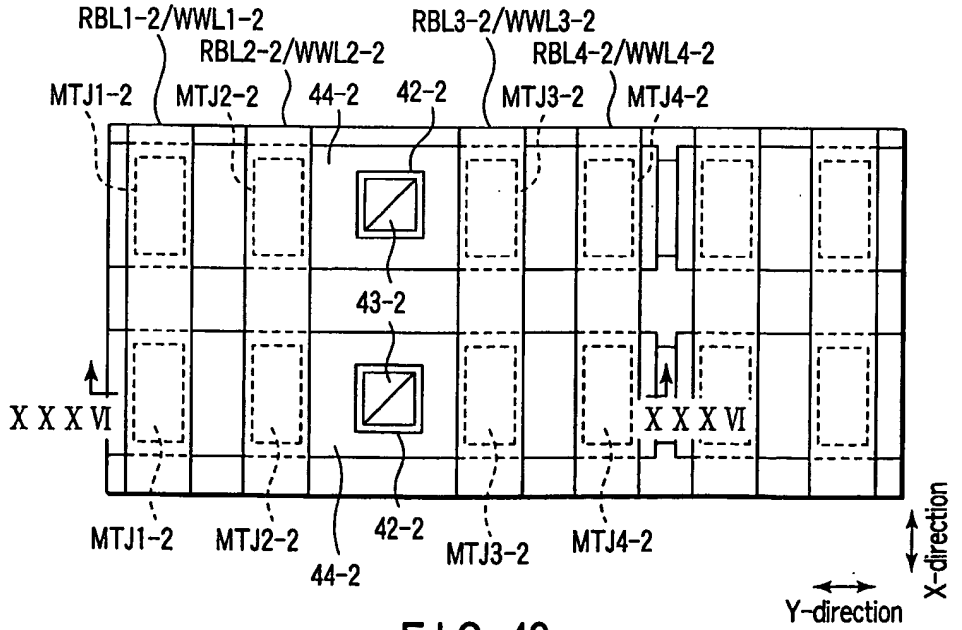
RBL1-2/WWL1-2
RBL2-2/WWL2-2
RBL3-2/WWL3-2
RBL4-2/WWL4-2
MTJ1-2
MTJ2-2
44-2
42-2
MTJ3-2
MTJ4-2
43-2
X X X VI
X X X VI
MTJ1-2
MTJ2-2
42-2
MTJ3-2
MTJ4-2
44-2
X-direction
Y-direction

FIG. 42

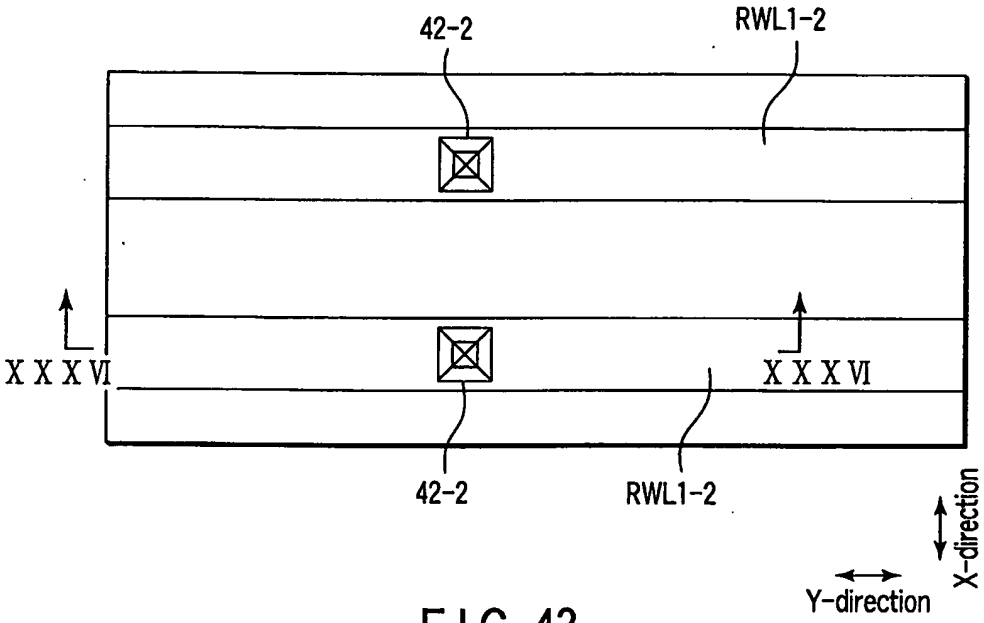

FIG. 43

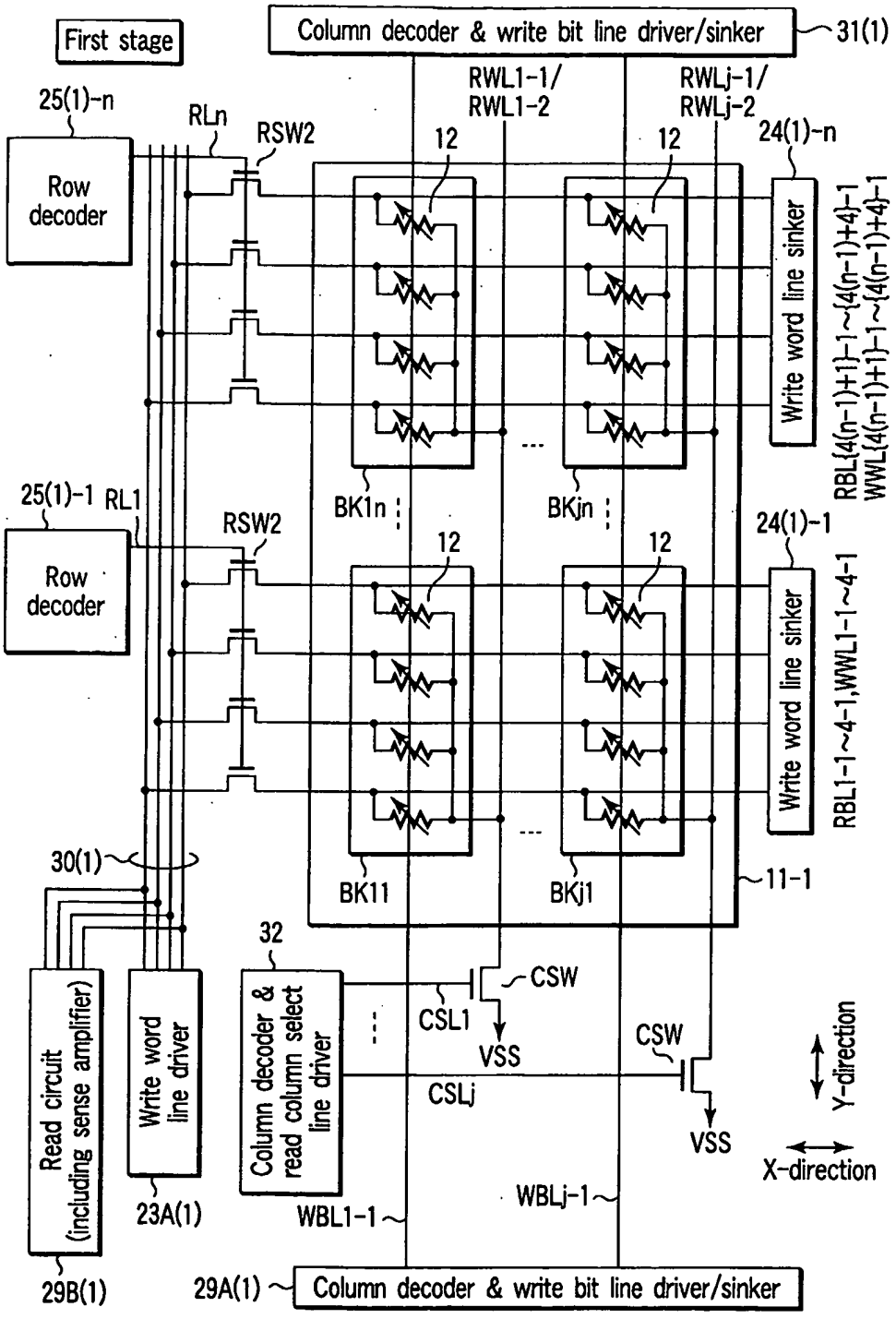
First stage
Column decoder & write bit line driver/sinker
31(1)
25(1)-n
RLn
RSW2
RWL1-1/
RWL1-2
RWLj-1/
RWLj-2
12
24(1)-n
Row decoder
Write word line sinker
RBL{4(n-1)+1}-1~{4(n-1)+4}-1
WWL{4(n-1)+1}-1~{4(n-1)+4}-1
25(1)-1
RL1
BK1n
BKjn
24(1)-1
RBL1-1~4-1,WWL1-1~4-1
30(1)
BK11
BKj1
11-1
32
CSW
CSL1
VSS
CSLj
Y-direction
X-direction
Read circuit (including sense amplifier)
Write word line driver
Column decoder & read column select line driver
23A(1)
WBL1-1
WBLj-1
29B(1)
29A(1)

FIG. 44

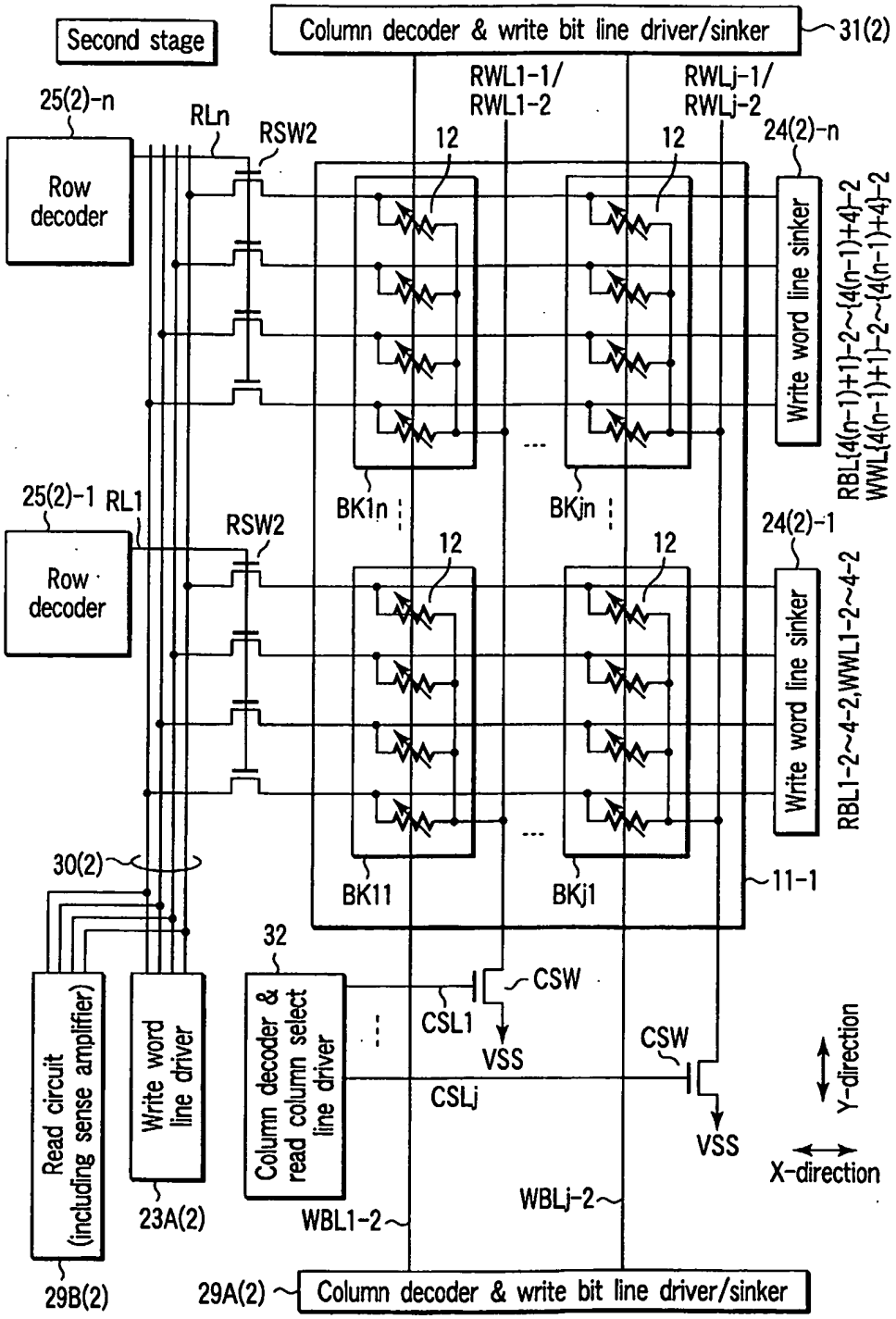
Second stage
Column decoder & write bit line driver/sinker
31(2)
RWL1-1/
RWL1-2
RWLj-1/
RWLj-2
25(2)-n
RLn
RSW2
12
24(2)-n
Row decoder
Write word line sinker
RBL{4(n-1)+1}-2~{4(n-1)+4}-2
WWL{4(n-1)+1}-2~{4(n-1)+4}-2
BK1n
BKjn
25(2)-1
RL1
RSW2
24(2)-1
RBL1-2~4-2,WWL1-2~4-2
BK11
BKj1
11-1
30(2)
32
CSW
CSL1
VSS
CSLj
Y-direction
X-direction
Read circuit (including sense amplifier)
Write word line driver
Column decoder & read column select line driver
23A(2)
WBL1-2
WBLj-2
29B(2)
29A(2)
Column decoder & write bit line driver/sinker

FIG. 45

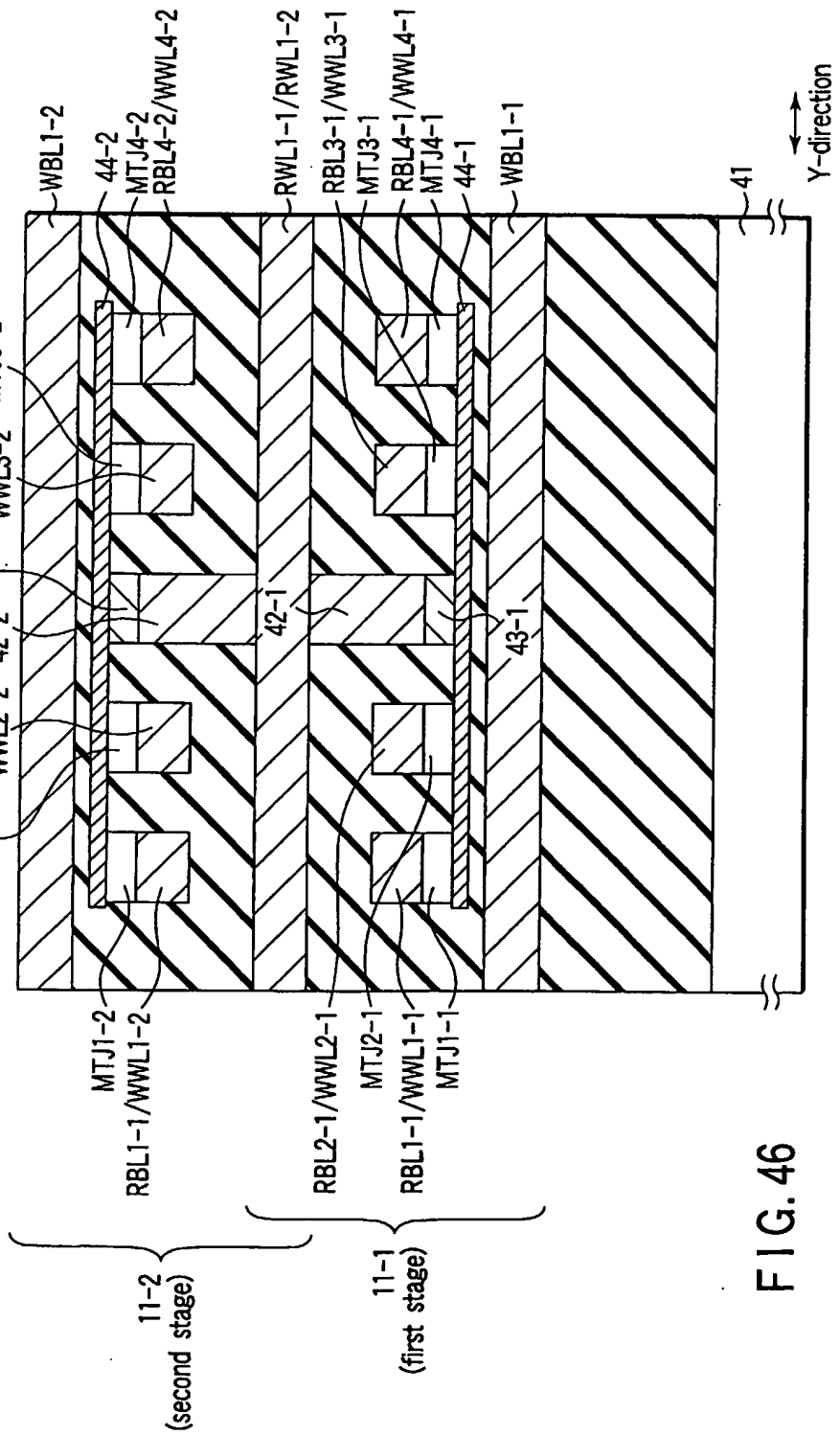
WBL1-2
44-2
MTJ4-2
RBL4-2/WWL4-2
RWL1-1/RWL1-2
RBL3-1/WWL3-1
MTJ3-1
RBL4-1/WWL4-1
MTJ4-1
44-1
WBL1-1
41
Y-direction
MTJ3-2
RBL3-2/
WWL3-2
43-2
42-2
RBL2-2/
WWL2-2
MTJ2-2
42-1
43-1
MTJ1-2
RBL1-1/WWL1-2
RBL2-1/WWL2-1
MTJ2-1
RBL1-1/WWL1-1
MTJ1-1
11-2
(second stage)
11-1
(first stage)

FIG. 46

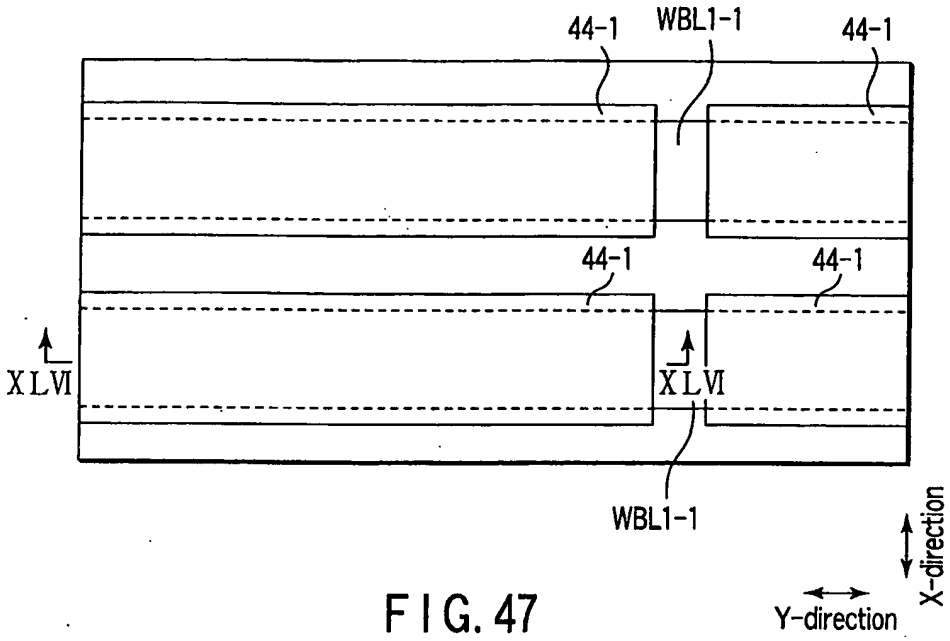
44-1
WBL1-1
44-1
44-1
44-1
XLVI
XLVI
WBL1-1
X-direction
Y-direction

FIG. 47

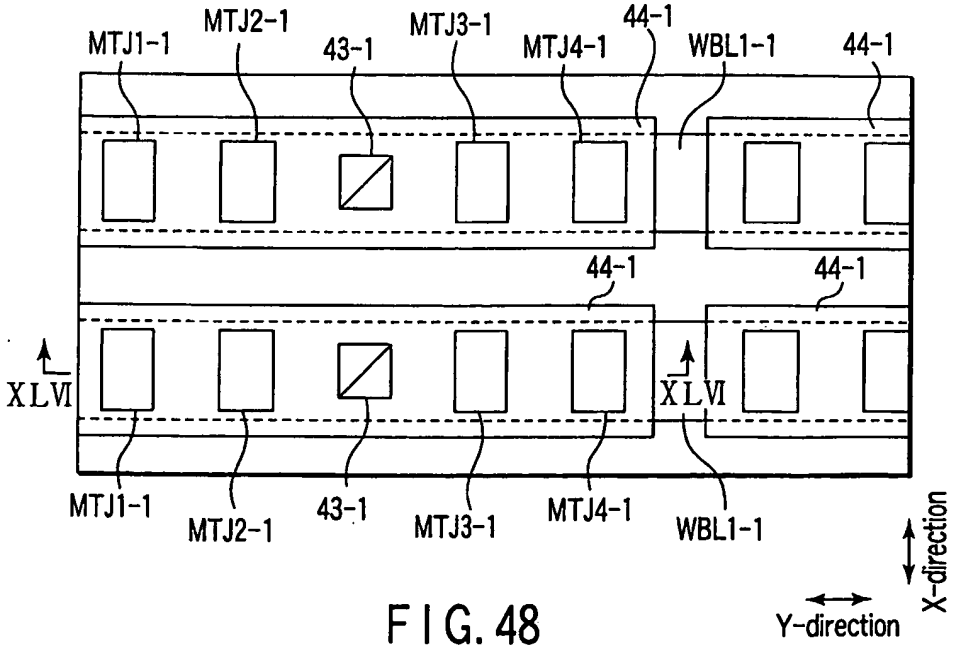
MTJ1-1
MTJ2-1
43-1
MTJ3-1
MTJ4-1
44-1
WBL1-1
44-1
44-1
44-1
XLVI
XLVI
MTJ1-1
MTJ2-1
43-1
MTJ3-1
MTJ4-1
WBL1-1
X-direction
Y-direction

FIG. 48

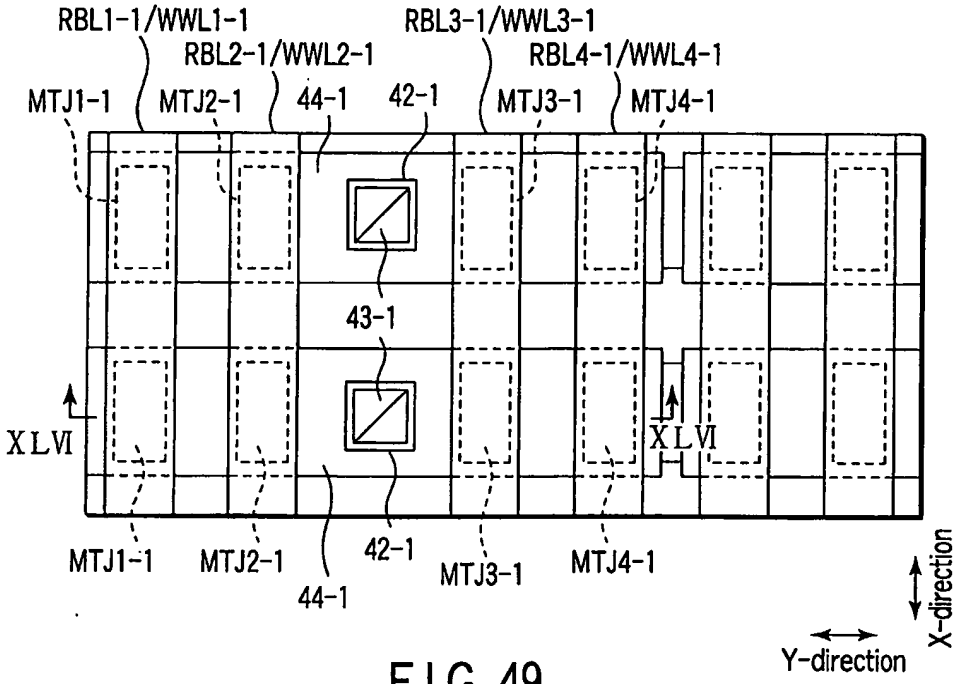
RBL1-1/WWL1-1
RBL2-1/WWL2-1
RBL3-1/WWL3-1
RBL4-1/WWL4-1
MTJ1-1
MTJ2-1
44-1
42-1
MTJ3-1
MTJ4-1
43-1
XLVI
XLVI
MTJ1-1
MTJ2-1
44-1
42-1
MTJ3-1
MTJ4-1
X-direction
Y-direction

FIG. 49

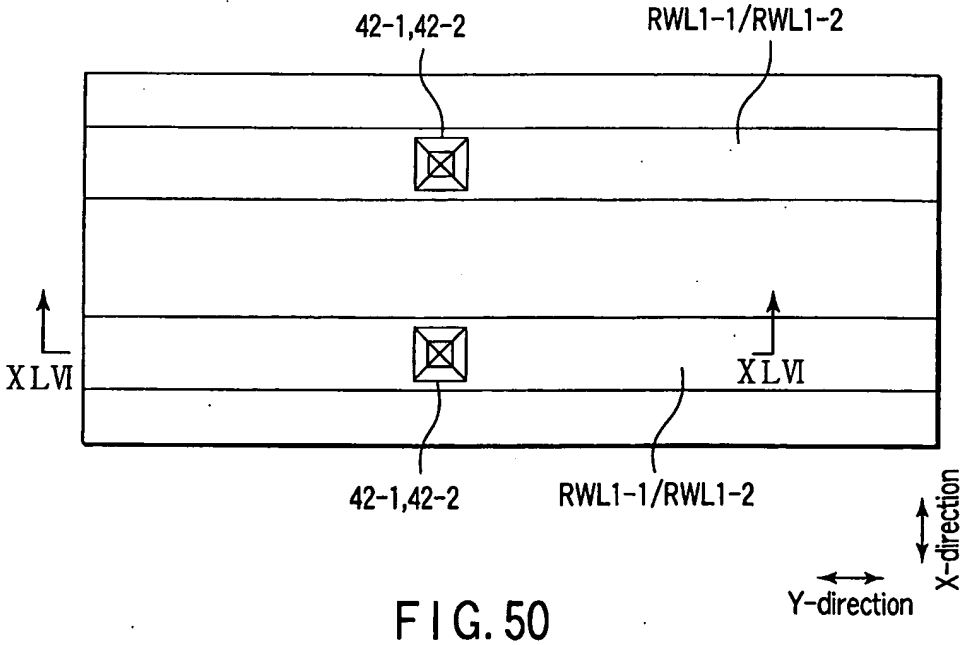
42-1,42-2
RWL1-1/RWL1-2
XLVI
XLVI
42-1,42-2
RWL1-1/RWL1-2
X-direction
Y-direction

FIG. 50

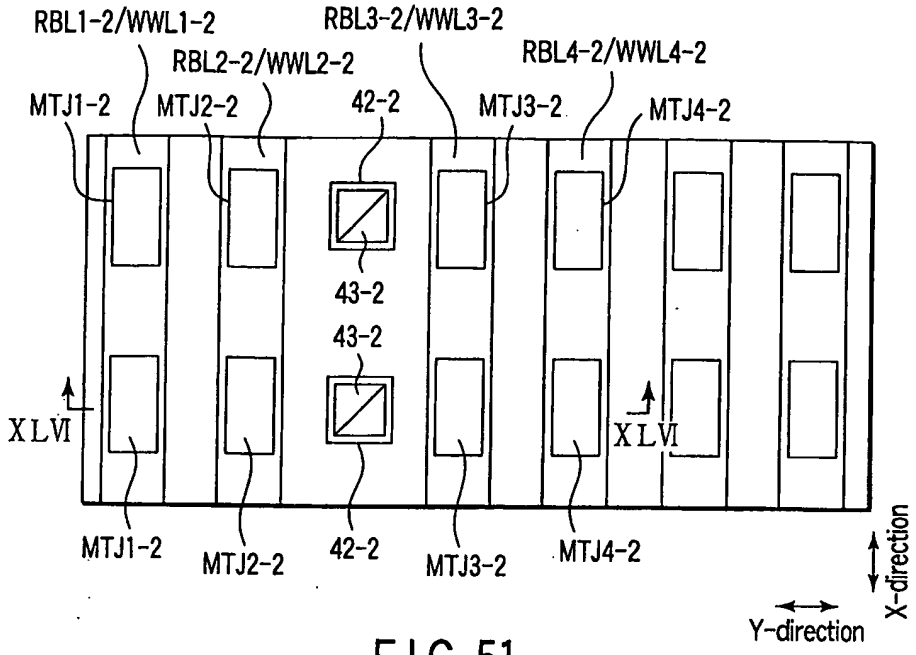
RBL1-2/WWL1-2
RBL2-2/WWL2-2
RBL3-2/WWL3-2
RBL4-2/WWL4-2
MTJ1-2
MTJ2-2
42-2
MTJ3-2
MTJ4-2
43-2
43-2
XLVI
XLVI
MTJ1-2
MTJ2-2
42-2
MTJ3-2
MTJ4-2
X-direction
Y-direction

FIG. 51

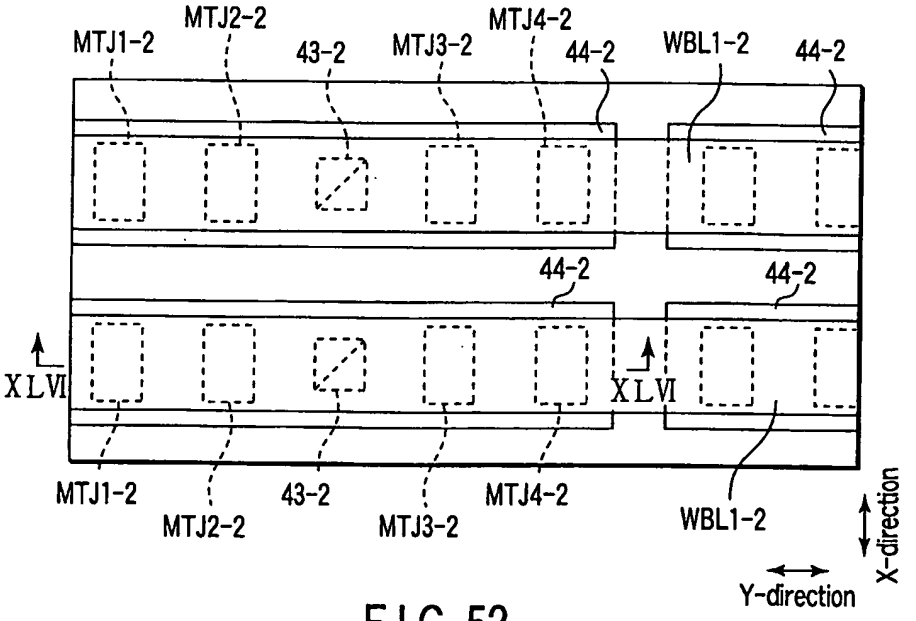
MTJ1-2
MTJ2-2
43-2
MTJ3-2
MTJ4-2
44-2
WBL1-2
44-2
44-2
44-2
XLVI
XLVI
MTJ1-2
MTJ2-2
43-2
MTJ3-2
MTJ4-2
WBL1-2
X-direction
Y-direction

FIG. 52

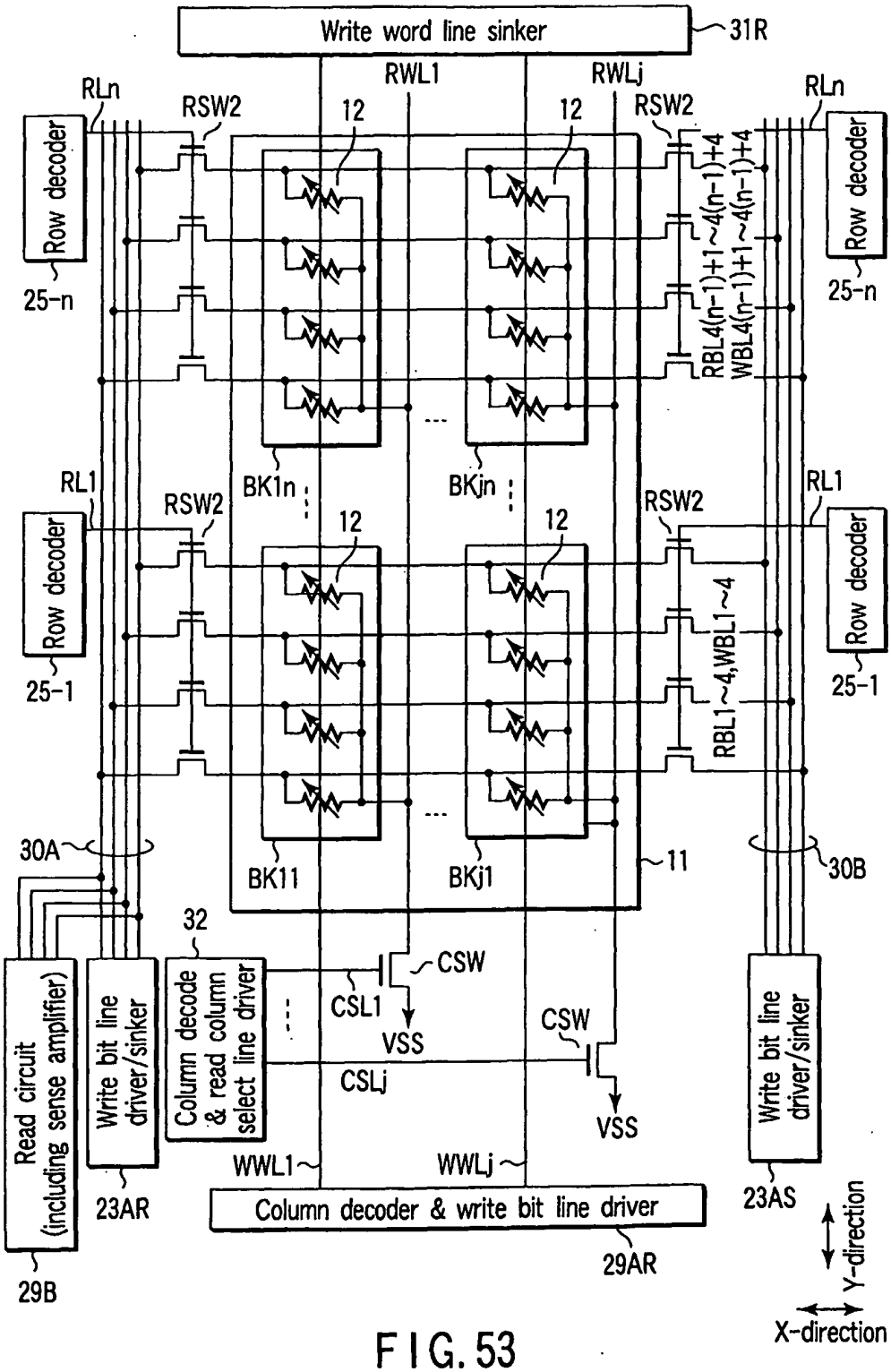
Write word line sinker
31R
RWL1
RWLj
RLn
RSW2
12
Row decoder
25-n
RBL4(n-1)+1~4(n-1)+4
WBL4(n-1)+1~4(n-1)+4
RL1
BK1n
BKjn
RBL1~4,WBL1~4
25-1
30A
30B
BK11
BKj1
11
32
Read circuit (including sense amplifier)
Write bit line driver/sinker
Column decode & read column select line driver
CSW
CSL1
CSLj
VSS
WWL1
WWLj
23AR
23AS
Column decoder & write bit line driver
29AR
29B
Y-direction
X-direction

FIG. 53

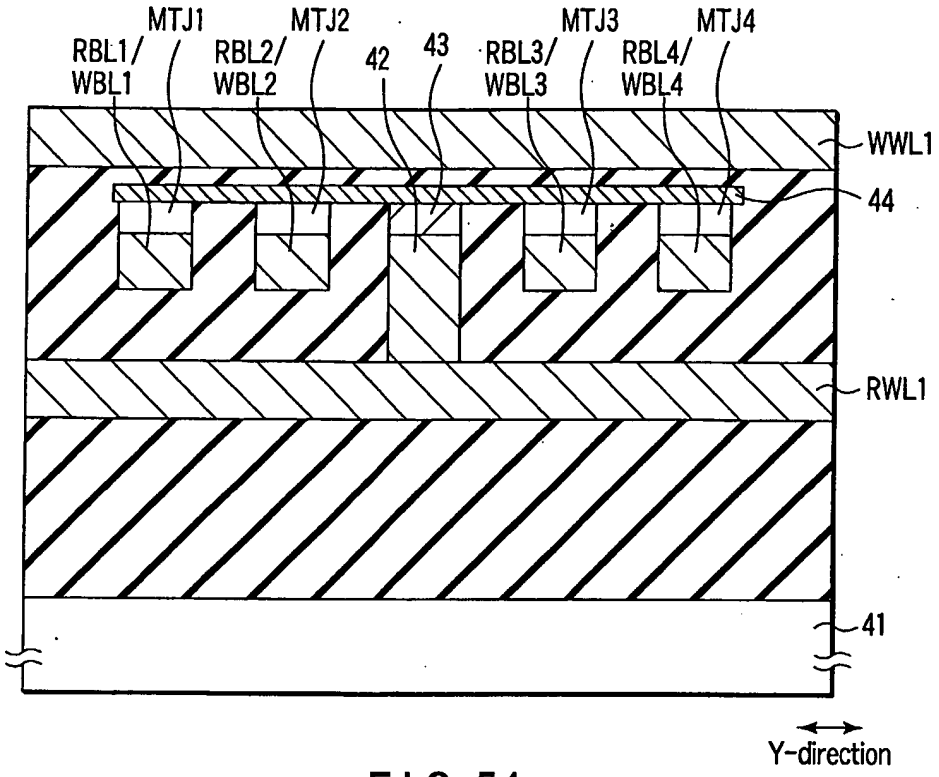
MTJ1
MTJ2
MTJ3
MTJ4
RBL1/
WBL1
RBL2/
WBL2
42
43
RBL3/
WBL3
RBL4/
WBL4
WWL1
44
RWL1
41
Y-direction

FIG. 54

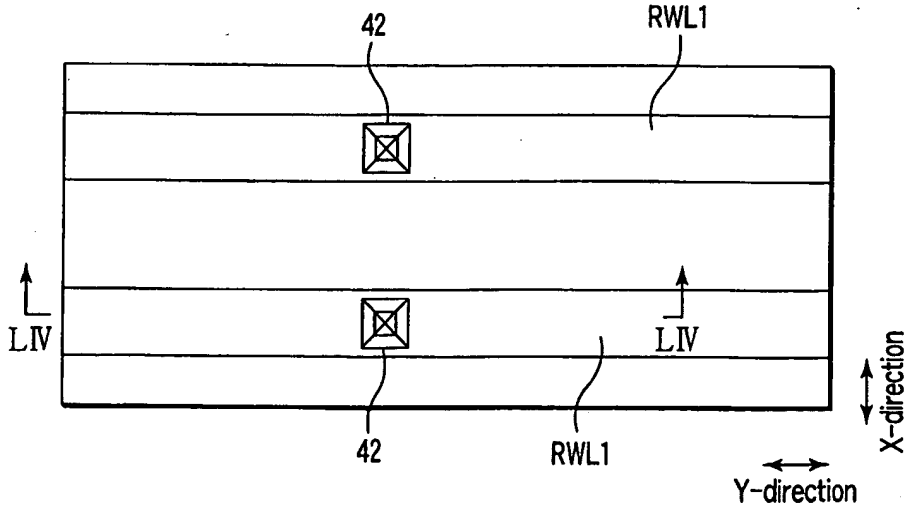
42
RWL1
LIV
LIV
42
RWL1
X-direction
Y-direction

FIG. 55

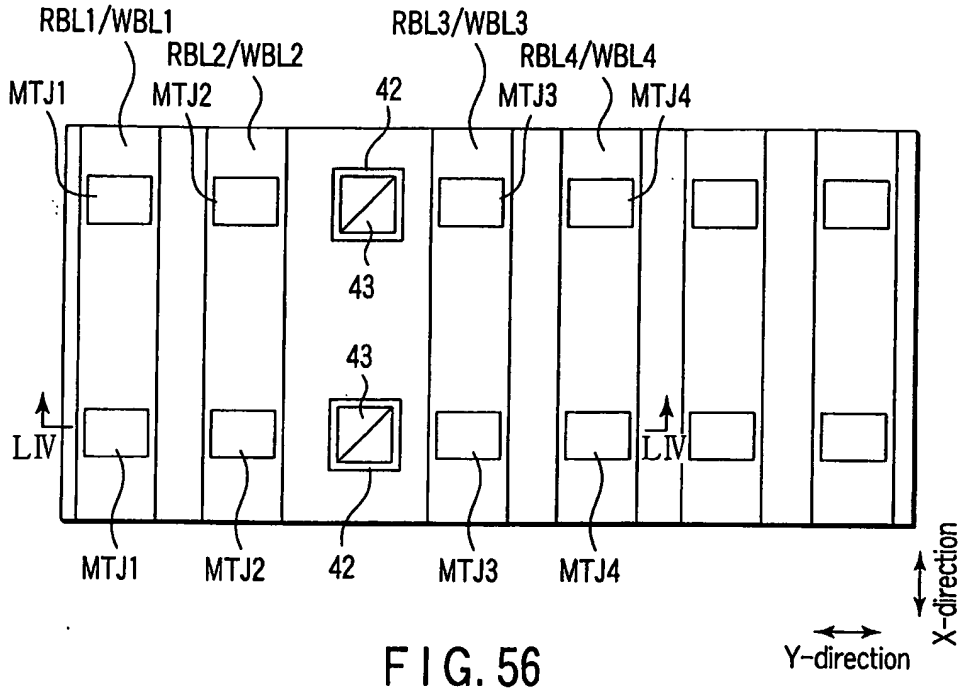
RBL1/WBL1
RBL2/WBL2
RBL3/WBL3
RBL4/WBL4
MTJ1
MTJ2
42
MTJ3
MTJ4
43
43
LIV
LIV
MTJ1
MTJ2
42
MTJ3
MTJ4
X-direction
Y-direction

FIG. 56

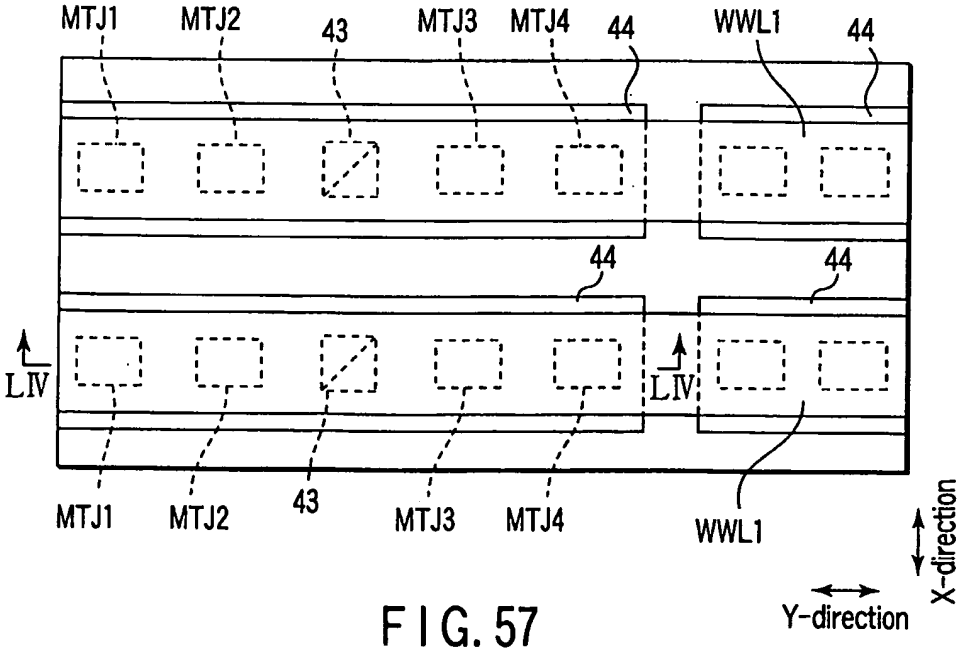
MTJ1
MTJ2
43
MTJ3
MTJ4
44
WWL1
44
44
44
LIV
LIV
MTJ1
MTJ2
43
MTJ3
MTJ4
WWL1
X-direction
Y-direction

FIG. 57

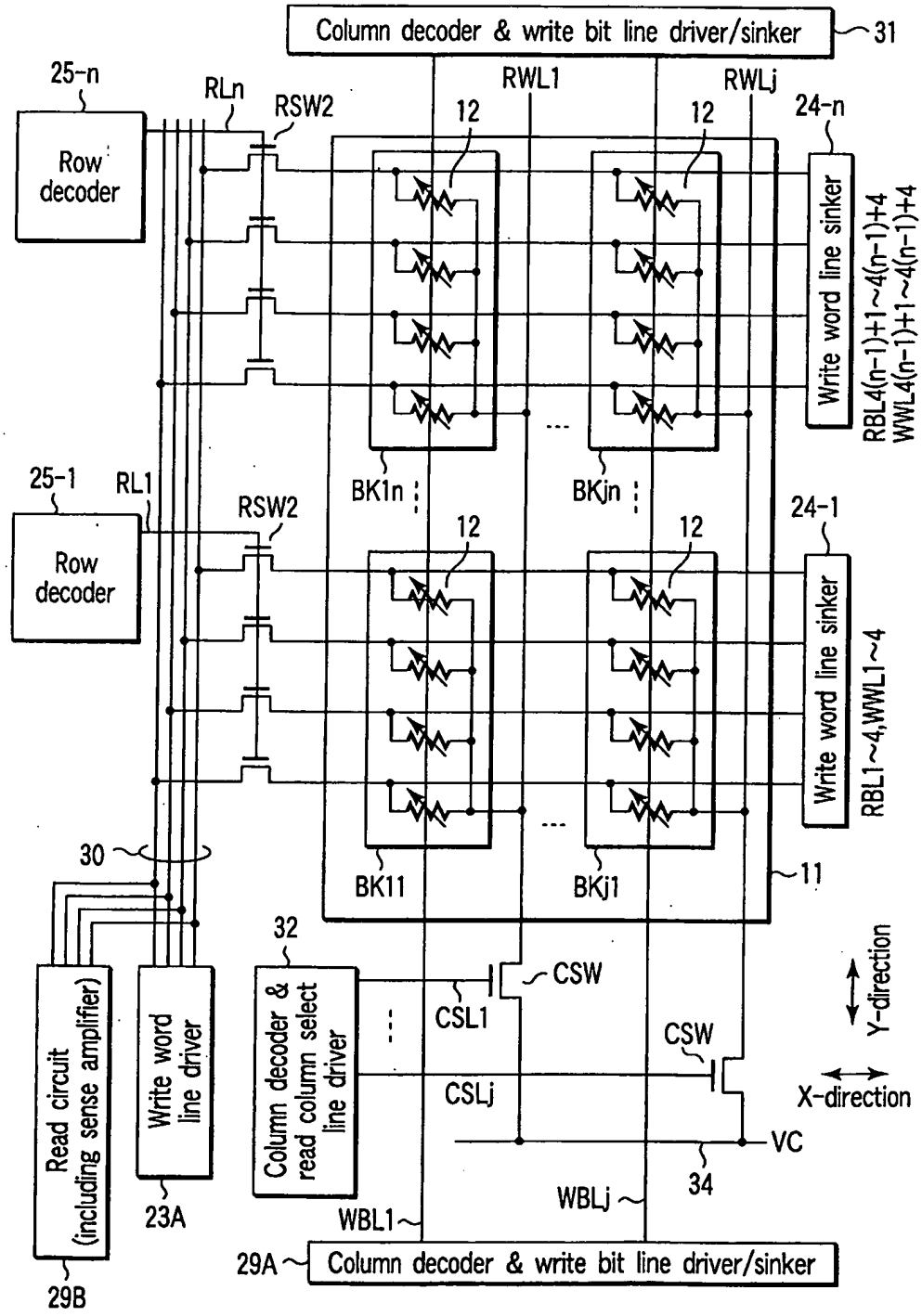
Column decoder & write bit line driver/sinker
31
25-n
Row decoder
RLn
RSW2
RWL1
RWLj
12
24-n
Write word line sinker
RBL4(n-1)+1~4(n-1)+4
WWL4(n-1)+1~4(n-1)+4
BK1n
BKjn
25-1
RL1
Row decoder
RSW2
24-1
Write word line sinker
RBL1~4,WWL1~4
30
BK11
BKj1
11
32
Read circuit (including sense amplifier)
Write word line driver
Column decoder & read column select line driver
CSW
CSL1
CSLj
Y-direction
X-direction
VC
34
WBL1
WBLj
23A
29A
29B
Column decoder & write bit line driver/sinker

FIG. 58

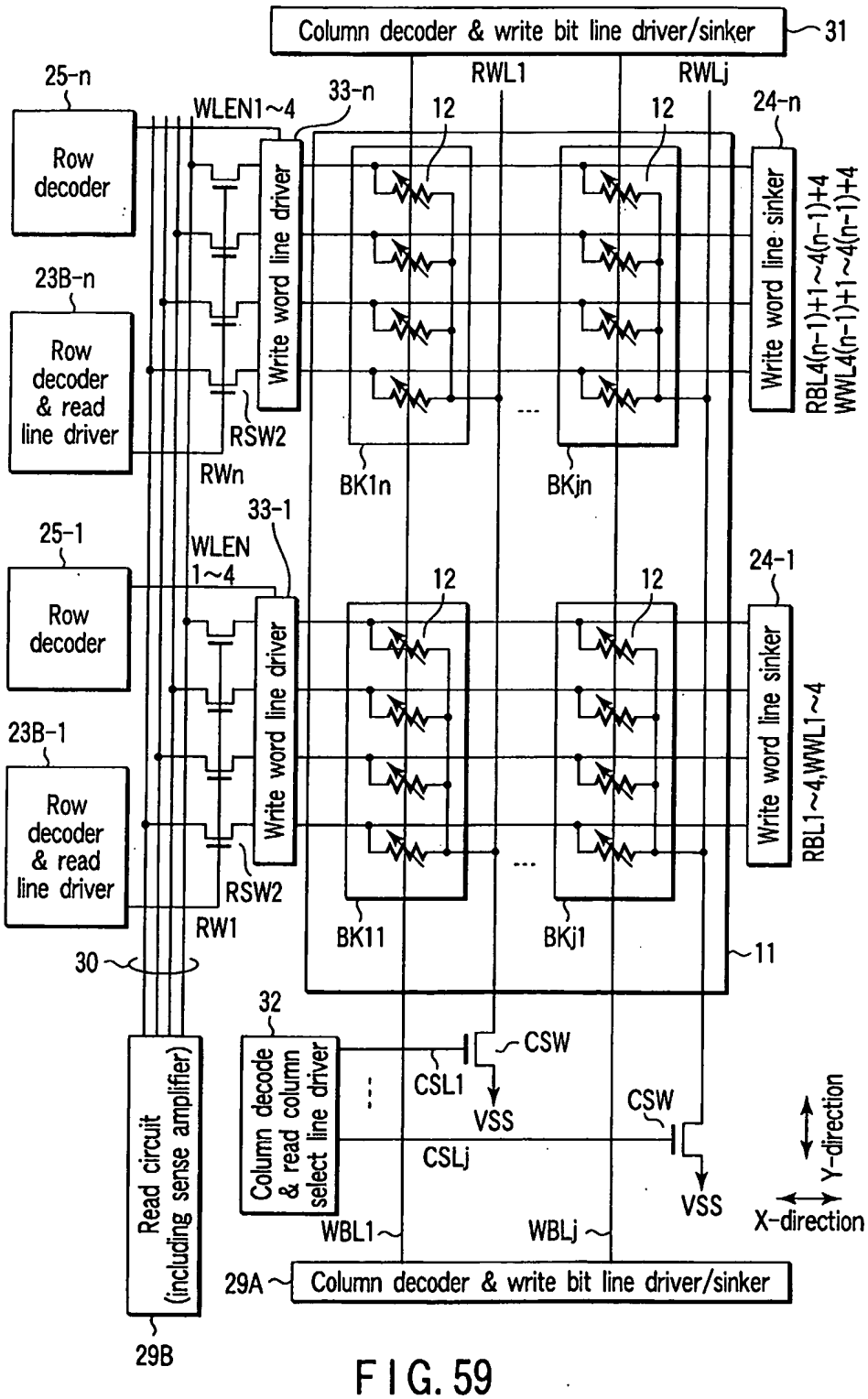
Column decoder & write bit line driver/sinker
31
25-n
Row decoder
WLEN1~4
33-n
Write word line driver
RWL1
RWLj
12
12
24-n
Write word line sinker
RBL4(n-1)+1~4(n-1)+4
WWL4(n-1)+1~4(n-1)+4
23B-n
Row decoder & read line driver
RSW2
RWn
BK1n
BKjn
25-1
Row decoder
WLEN 1~4
33-1
Write word line driver
12
12
24-1
Write word line sinker
RBL1~4,WWL1~4
23B-1
Row decoder & read line driver
RSW2
RW1
BK11
BKj1
11
30
32
Column decode & read column select line driver
CSW
CSL1
VSS
CSW
CSLj
VSS
Y-direction
X-direction
Read circuit (including sense amplifier)
WBL1
WBLj
29A
Column decoder & write bit line driver/sinker
29B

FIG. 59

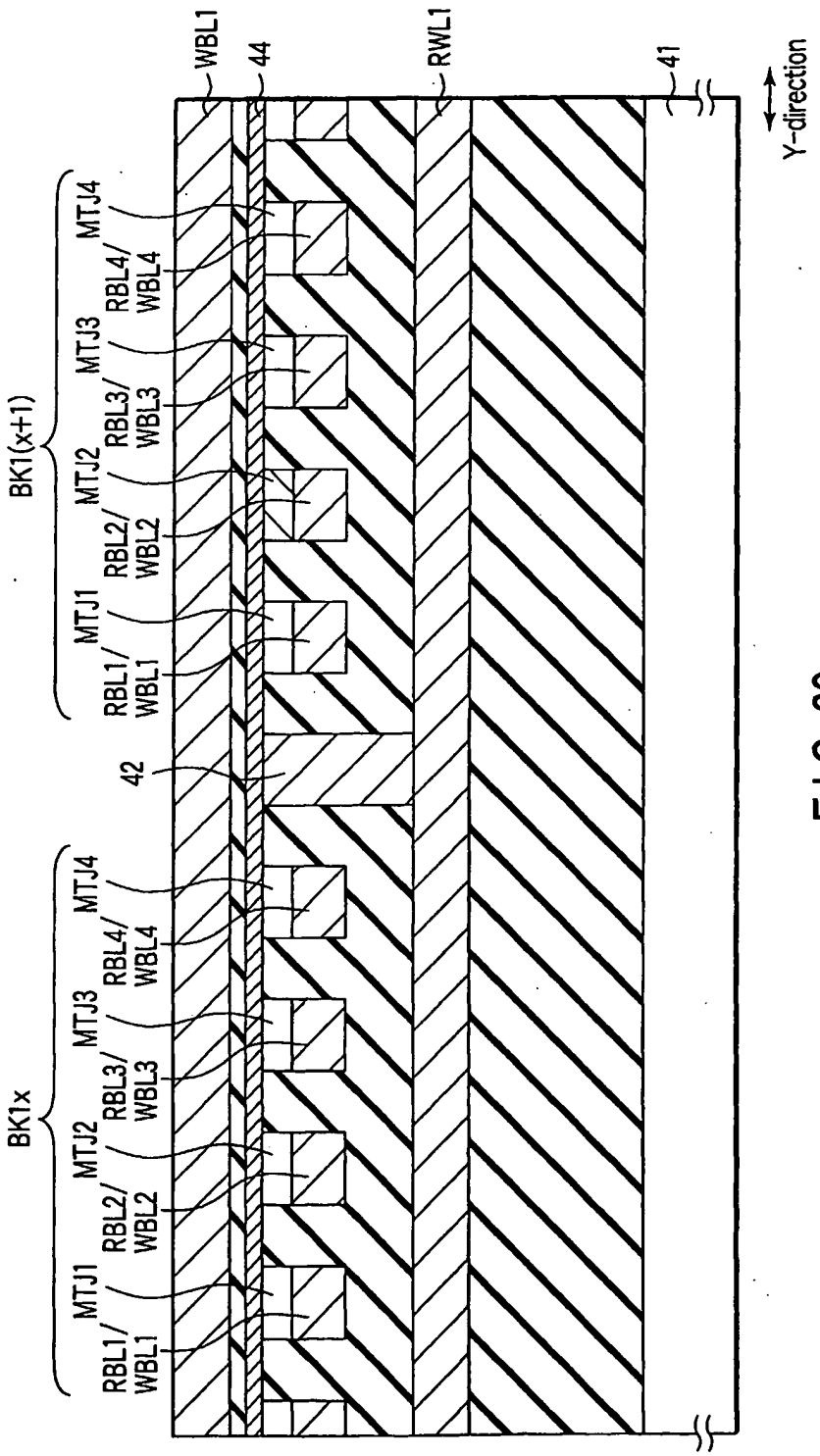
WBL1
44
RWL1
41
Y-direction
BK1(x+1)
BK1x
MTJ1
RBL1/
WBL1
MTJ2
RBL2/
WBL2
MTJ3
RBL3/
WBL3
MTJ4
RBL4/
WBL4
42

FIG. 60

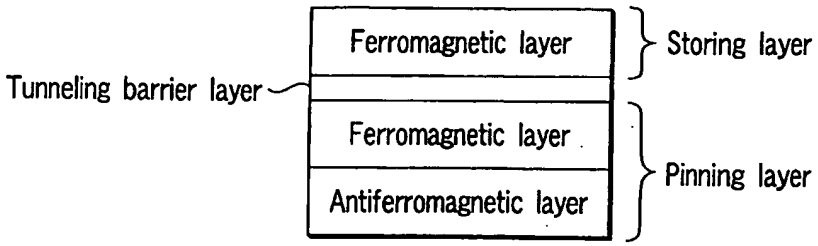

FIG. 61

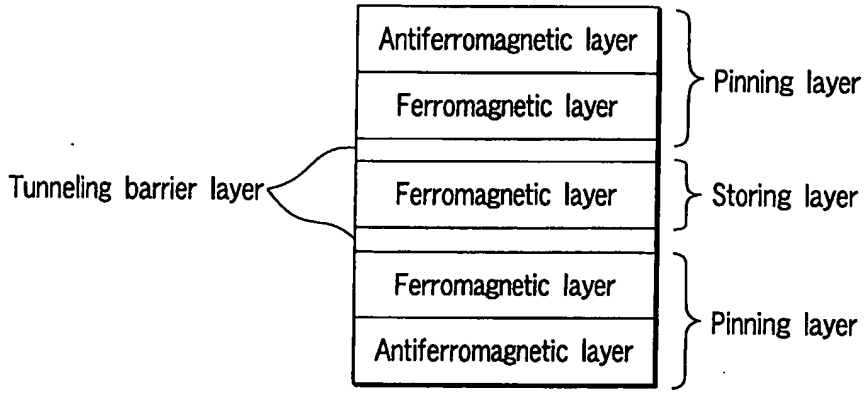

FIG. 62

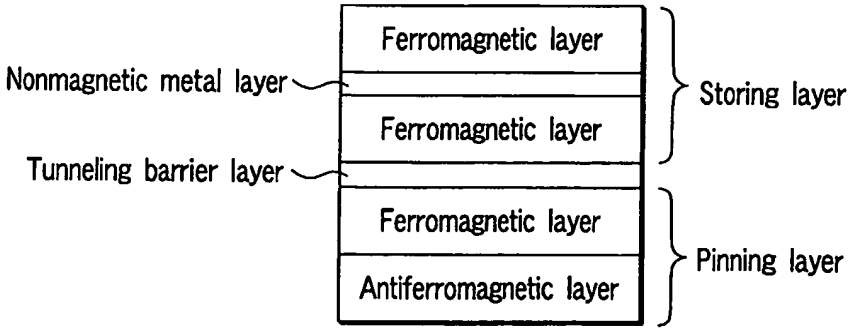

FIG. 63

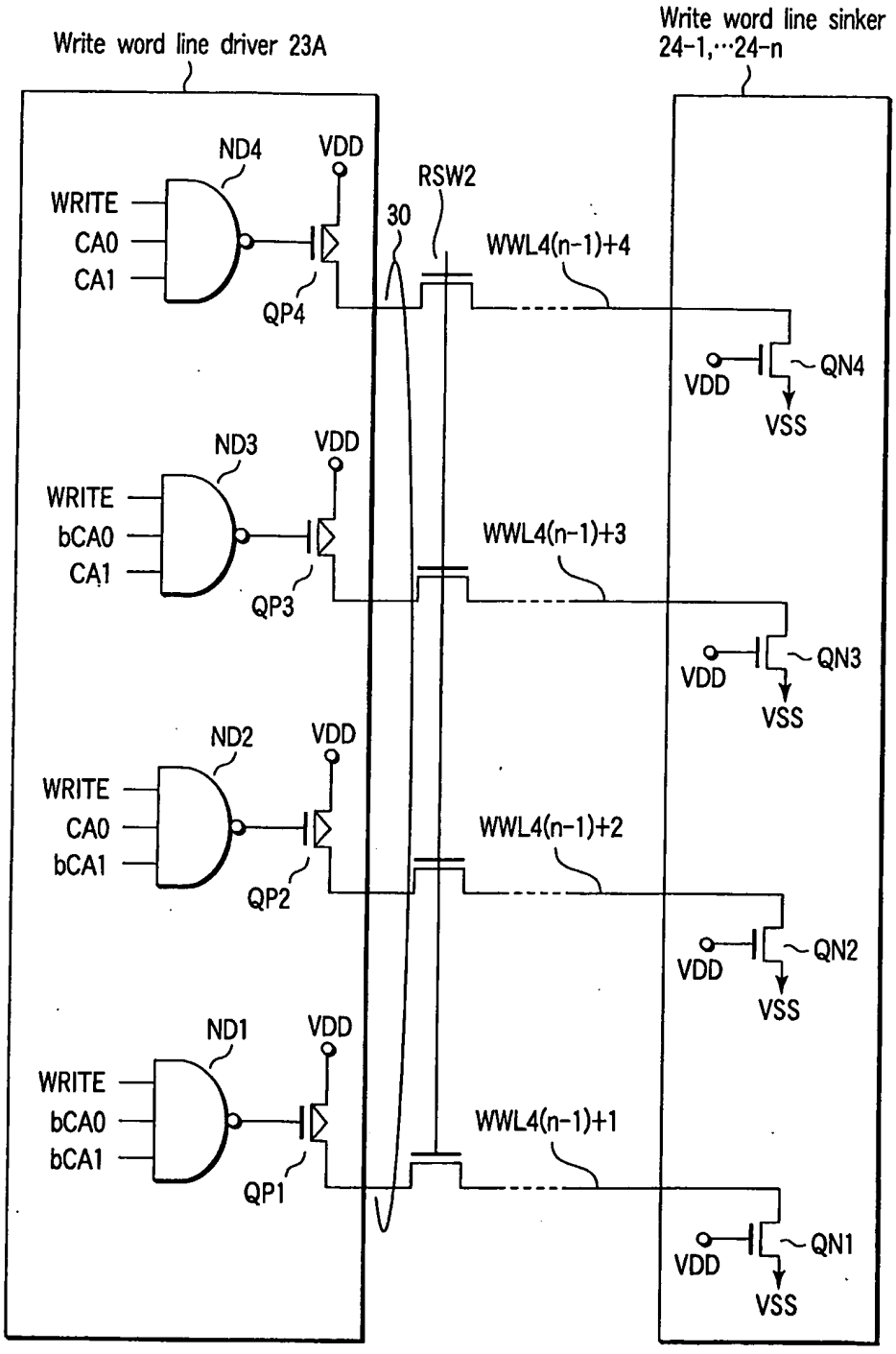
Write word line driver 23A
Write word line sinker 24-1,···24-n
ND4
VDD
RSW2
WRITE
CA0
CA1
30
WWL4(n-1)+4
QP4
VDD
QN4
VSS
ND3
VDD
WRITE
bCA0
CA1
WWL4(n-1)+3
QP3
VDD
QN3
VSS
ND2
VDD
WRITE
CA0
bCA1
WWL4(n-1)+2
QP2
VDD
QN2
VSS
ND1
VDD
WRITE
bCA0
bCA1
WWL4(n-1)+1
QP1
VDD
QN1
VSS

FIG. 64

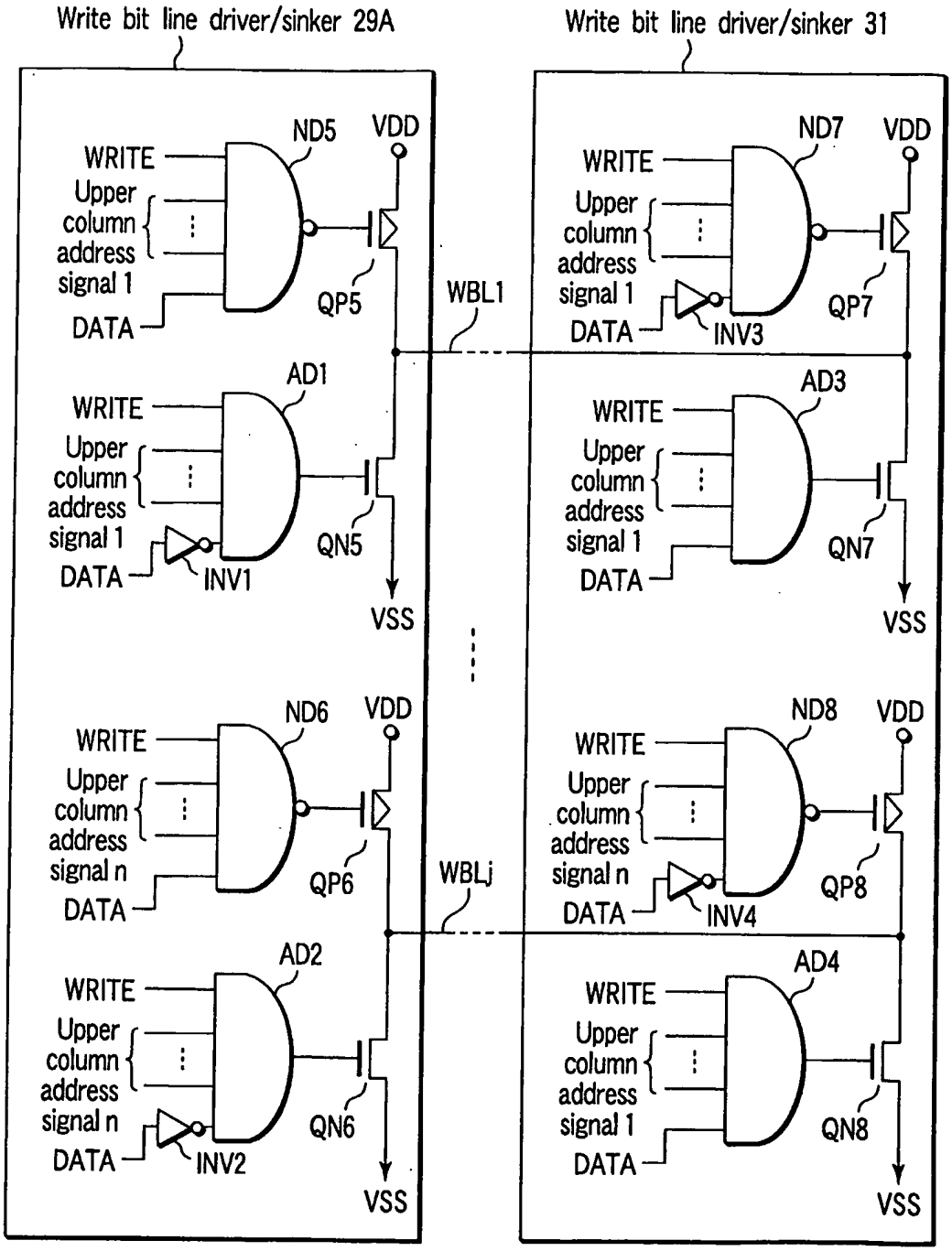
Write bit line driver/sinker 29A
Write bit line driver/sinker 31
WRITE
Upper column address signal 1
DATA
ND5
VDD
QP5
WBL1
ND7
QP7
INV3
AD1
QN5
INV1
AD3
QN7
VSS
ND6
QP6
WBLj
ND8
QP8
INV4
AD2
QN6
INV2
AD4
QN8
Upper column address signal n

FIG. 65

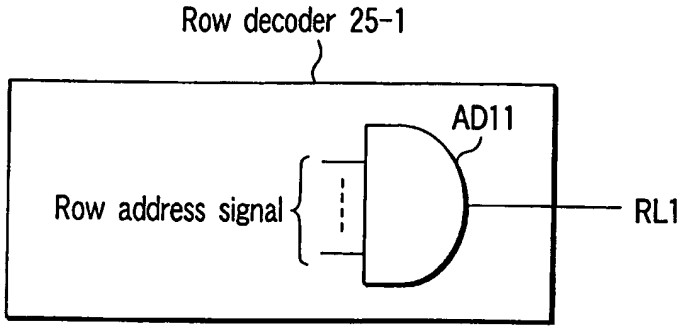
Row decoder 25-1
AD11
Row address signal
RL1

FIG. 66

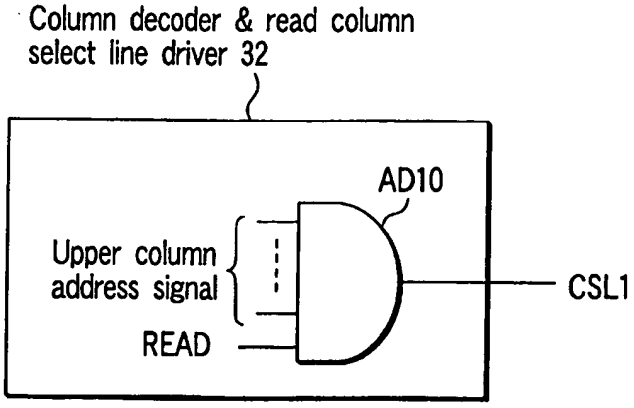
Column decoder & read column
select line driver 32
AD10
Upper column
address signal
READ
CSL1

FIG. 67

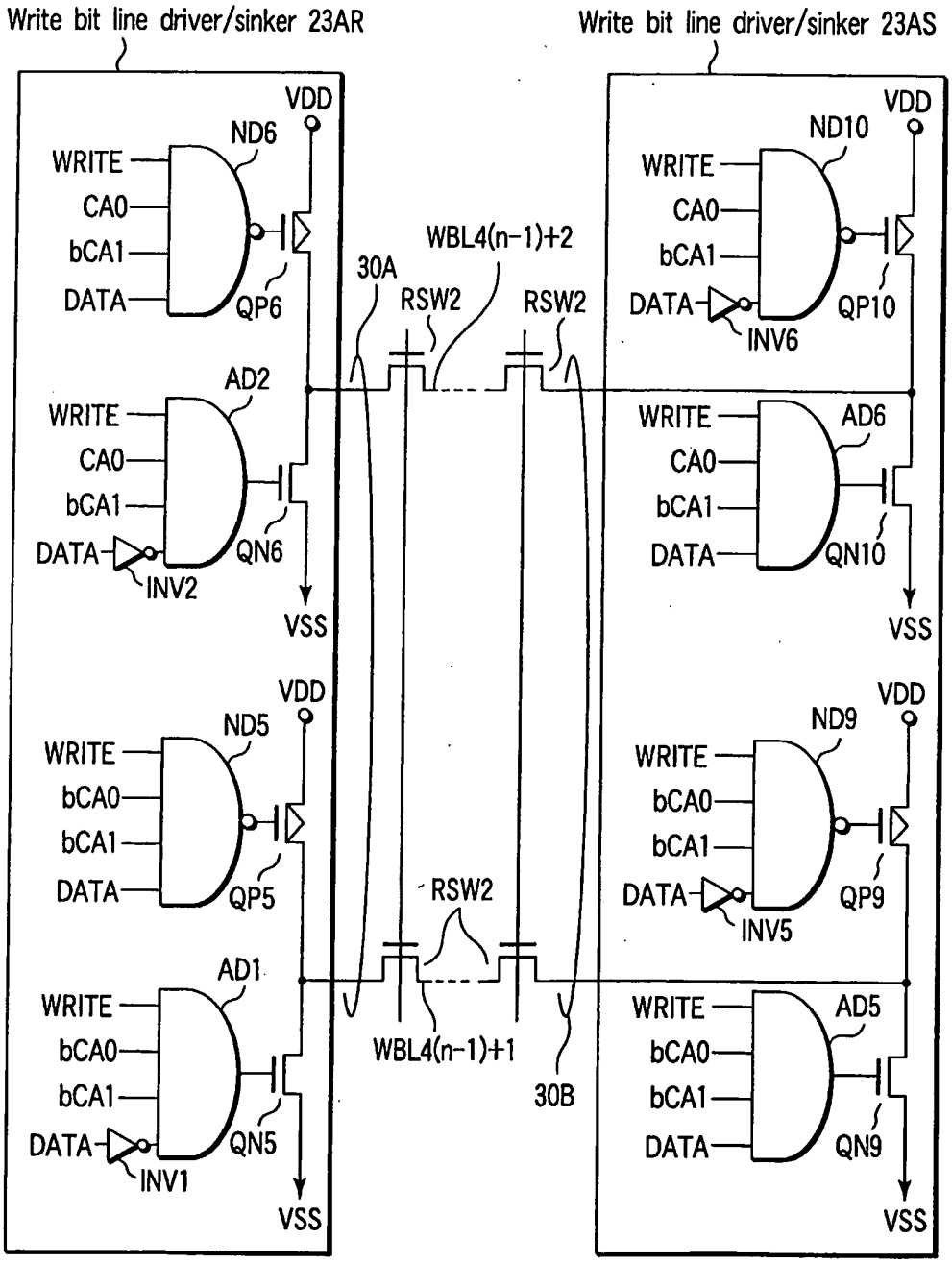
Write bit line driver/sinker 23AR
Write bit line driver/sinker 23AS
VDD
ND6
WRITE
CA0
bCA1
DATA
QP6
AD2
QN6
INV2
VSS
ND5
bCA0
QP5
AD1
QN5
INV1
WBL4(n-1)+2
30A
RSW2
30B
WBL4(n-1)+1
ND10
QP10
INV6
AD6
QN10
ND9
QP9
INV5
AD5
QN9

FIG. 68

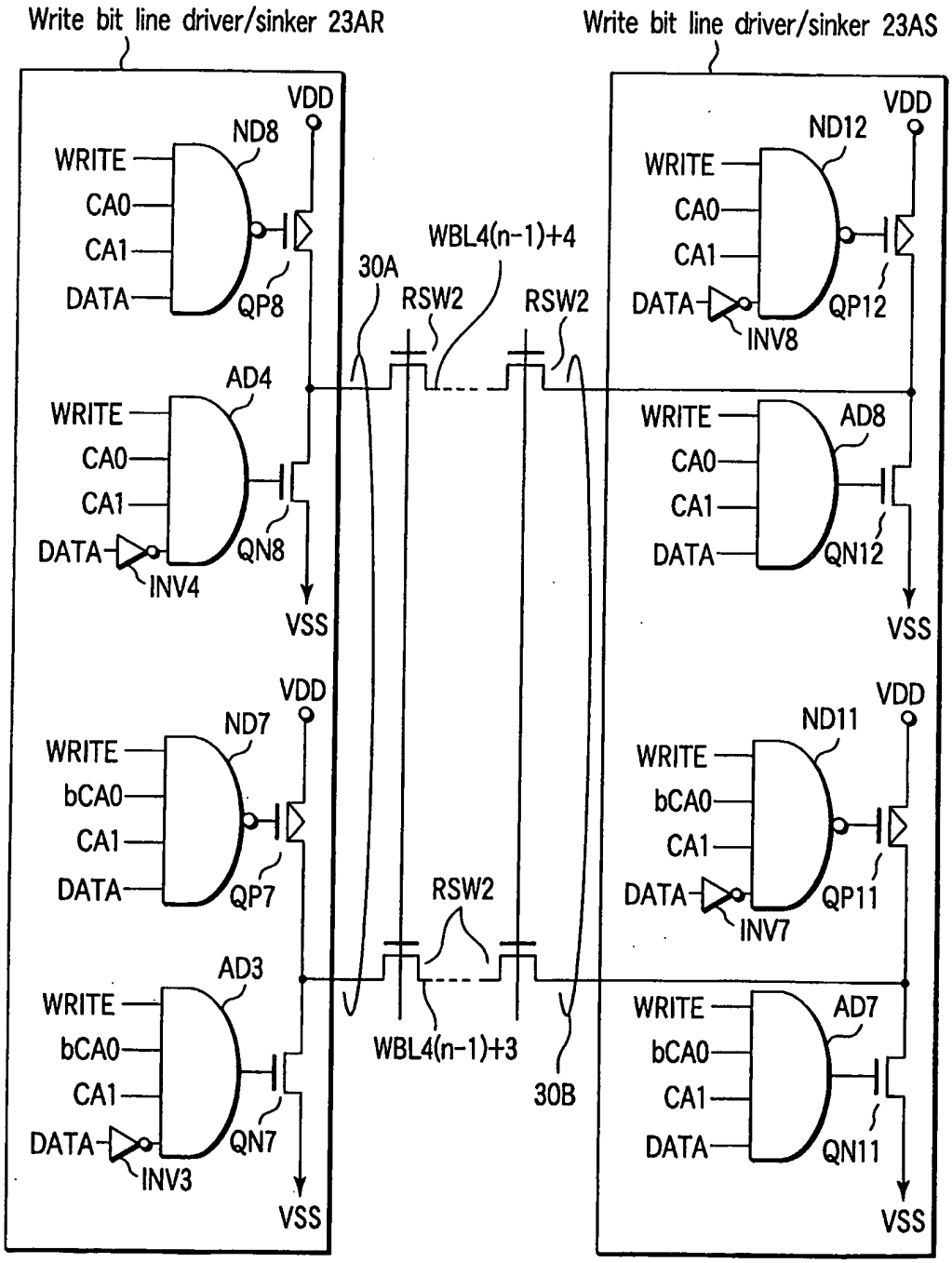
Write bit line driver/sinker 23AR
Write bit line driver/sinker 23AS
VDD
ND8
WRITE
CA0
CA1
DATA
QP8
30A
WBL4(n-1)+4
RSW2
RSW2
ND12
QP12
INV8
AD4
QN8
INV4
VSS
AD8
QN12
ND7
bCA0
QP7
ND11
QP11
INV7
AD3
QN7
INV3
WBL4(n-1)+3
30B
AD7
QN11

FIG. 69

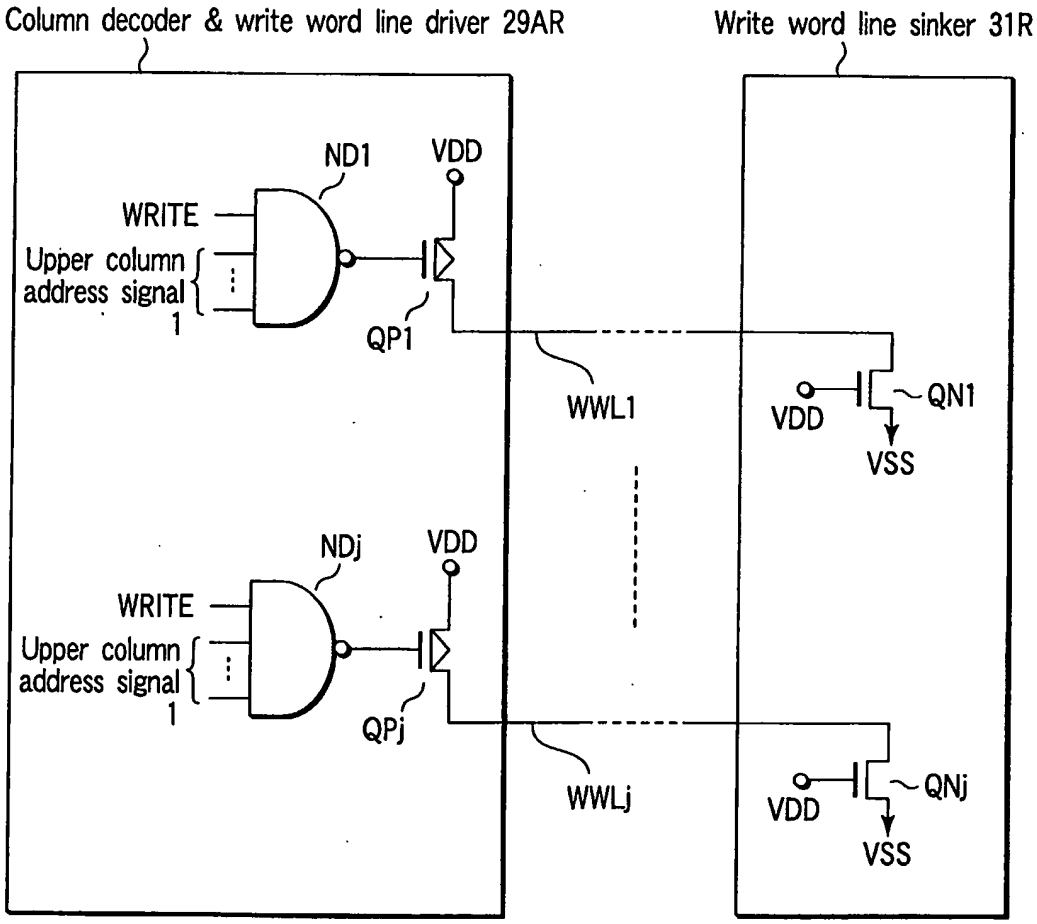
Column decoder & write word line driver 29AR
Write word line sinker 31R
ND1
VDD
WRITE
Upper column address signal 1
QP1
WWL1
QN1
VDD
VSS
NDj
VDD
WRITE
Upper column address signal 1
QPj
WWLj
QNj
VDD
VSS

FIG. 70

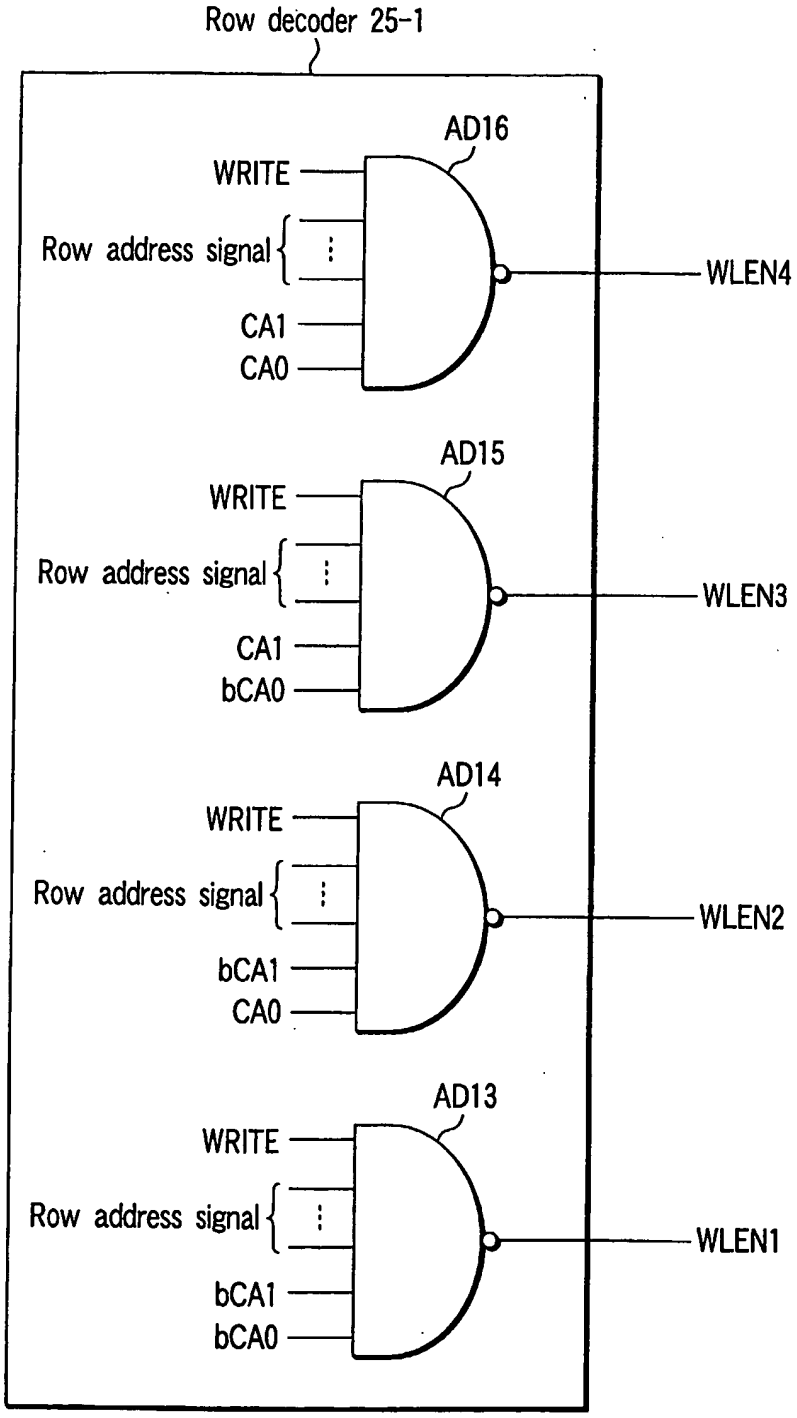
Row decoder 25-1
AD16
WRITE
Row address signal
CA1
CA0
WLEN4
AD15
WRITE
Row address signal
CA1
bCA0
WLEN3
AD14
WRITE
Row address signal
bCA1
CA0
WLEN2
AD13
WRITE
Row address signal
bCA1
bCA0
WLEN1

FIG. 71

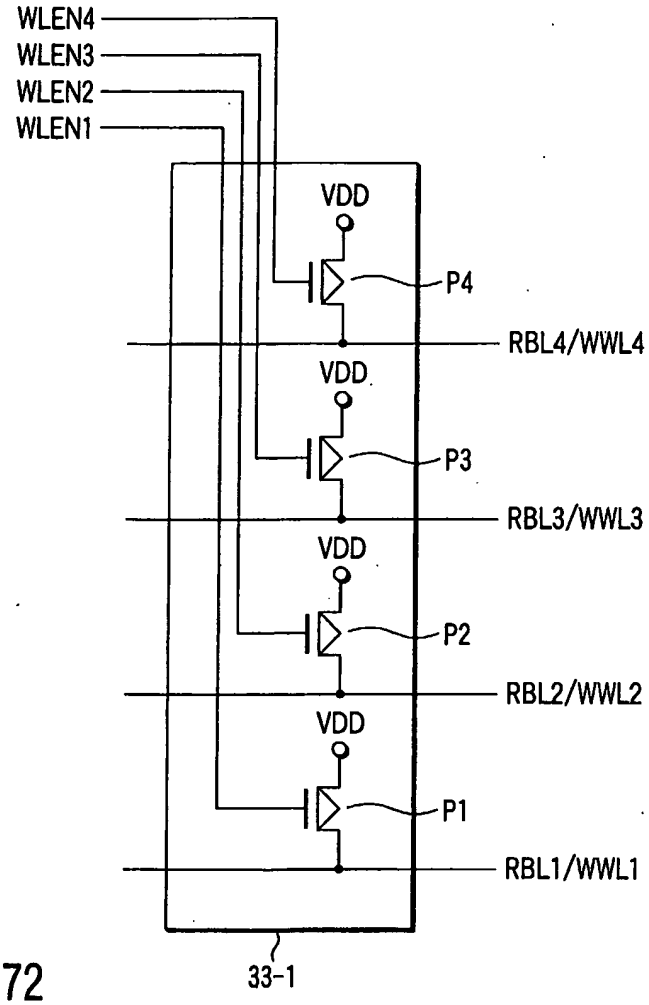
WLEN4
WLEN3
WLEN2
WLEN1
VDD
P4
RBL4/WWL4
VDD
P3
RBL3/WWL3
VDD
P2
RBL2/WWL2
VDD
P1
RBL1/WWL1
33-1

FIG. 72

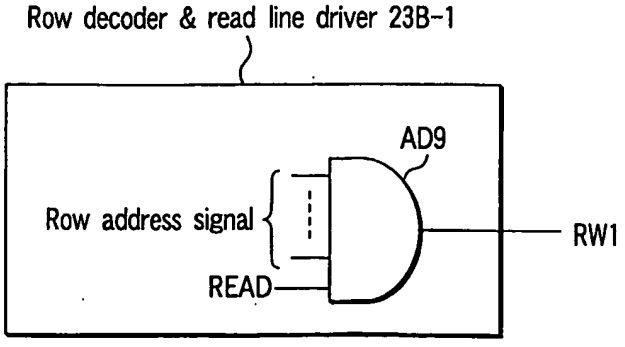
Row decoder & read line driver 23B-1
AD9
Row address signal
READ
RW1

FIG. 73

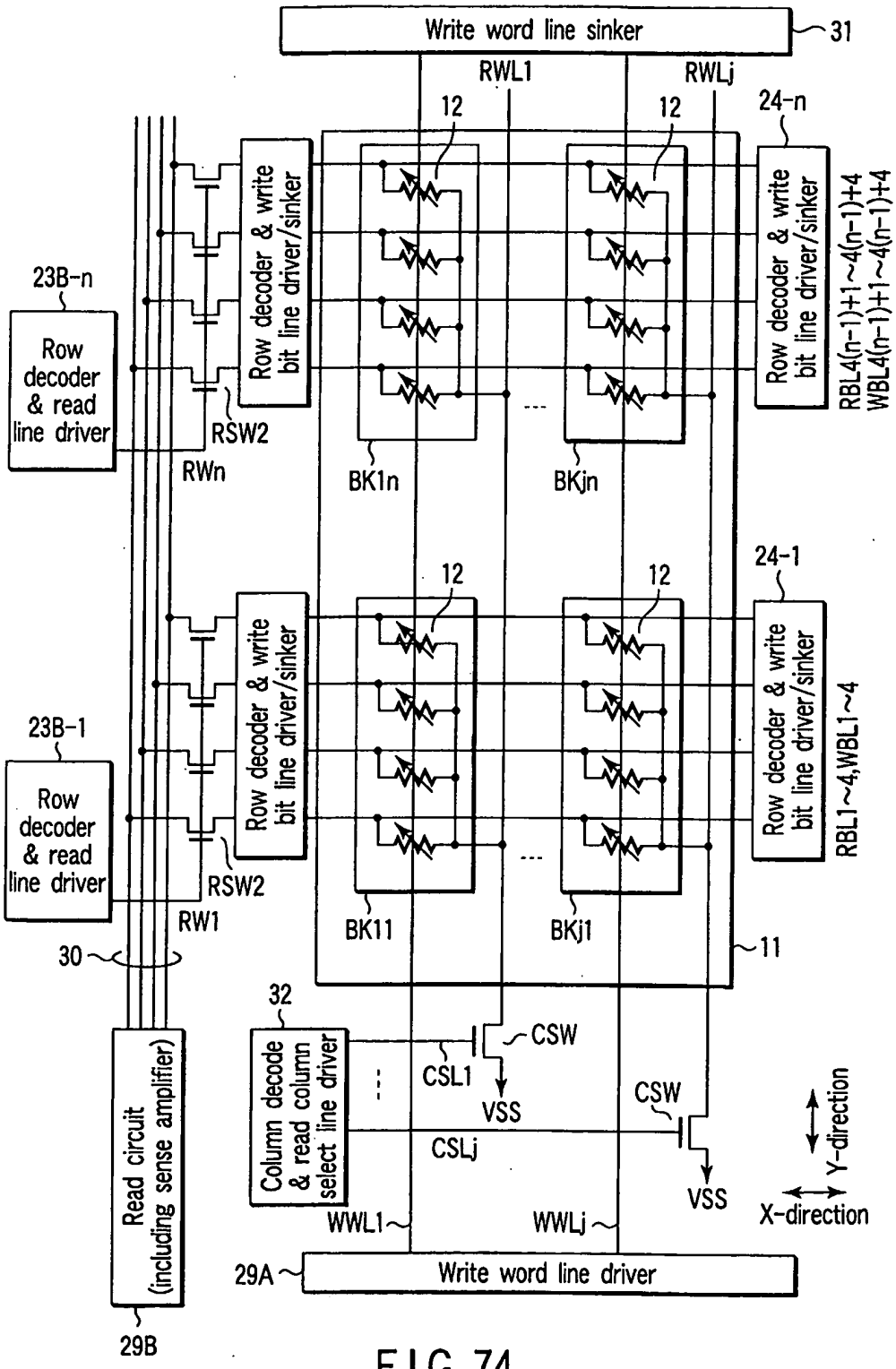
Write word line sinker
31
RWL1
RWLj
12
24-n
Row decoder & write bit line driver/sinker
RBL4(n-1)+1~4(n-1)+4
WBL4(n-1)+1~4(n-1)+4
23B-n
Row decoder & read line driver
RSW2
RWn
BK1n
BKjn
24-1
RBL1~4,WBL1~4
23B-1
RW1
BK11
BKj1
11
30
32
Column decode & read column select line driver
CSW
CSL1
VSS
CSLj
Y-direction
X-direction
WWL1
WWLj
29A
Write word line driver
Read circuit (including sense amplifier)
29B

FIG. 74

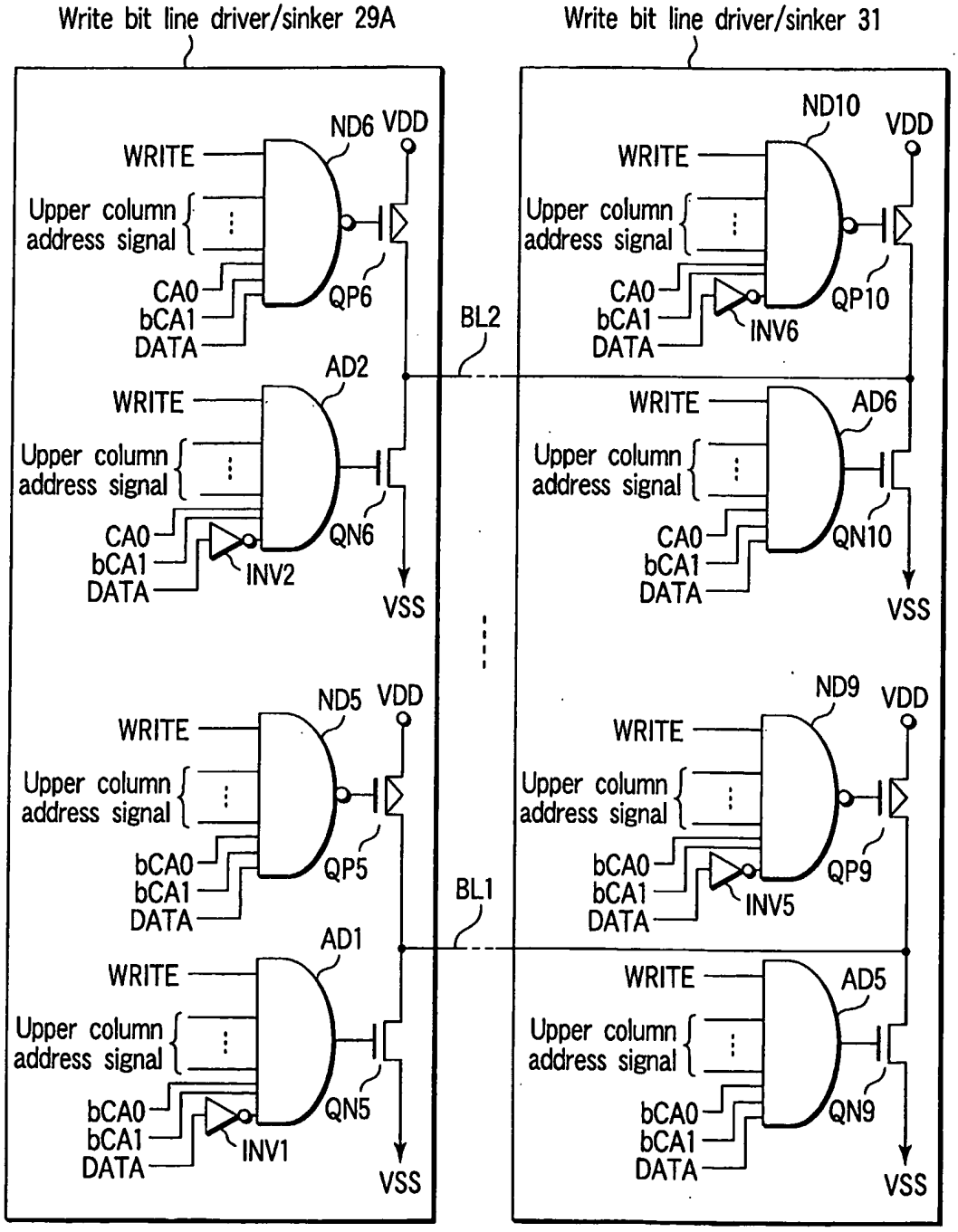
Write bit line driver/sinker 29A
Write bit line driver/sinker 31
ND6
VDD
WRITE
Upper column address signal
CA0
bCA1
DATA
QP6
BL2
AD2
QN6
INV2
VSS
ND10
QP10
INV6
AD6
QN10
ND5
bCA0
QP5
BL1
AD1
QN5
INV1
ND9
QP9
INV5
AD5
QN9

FIG. 75

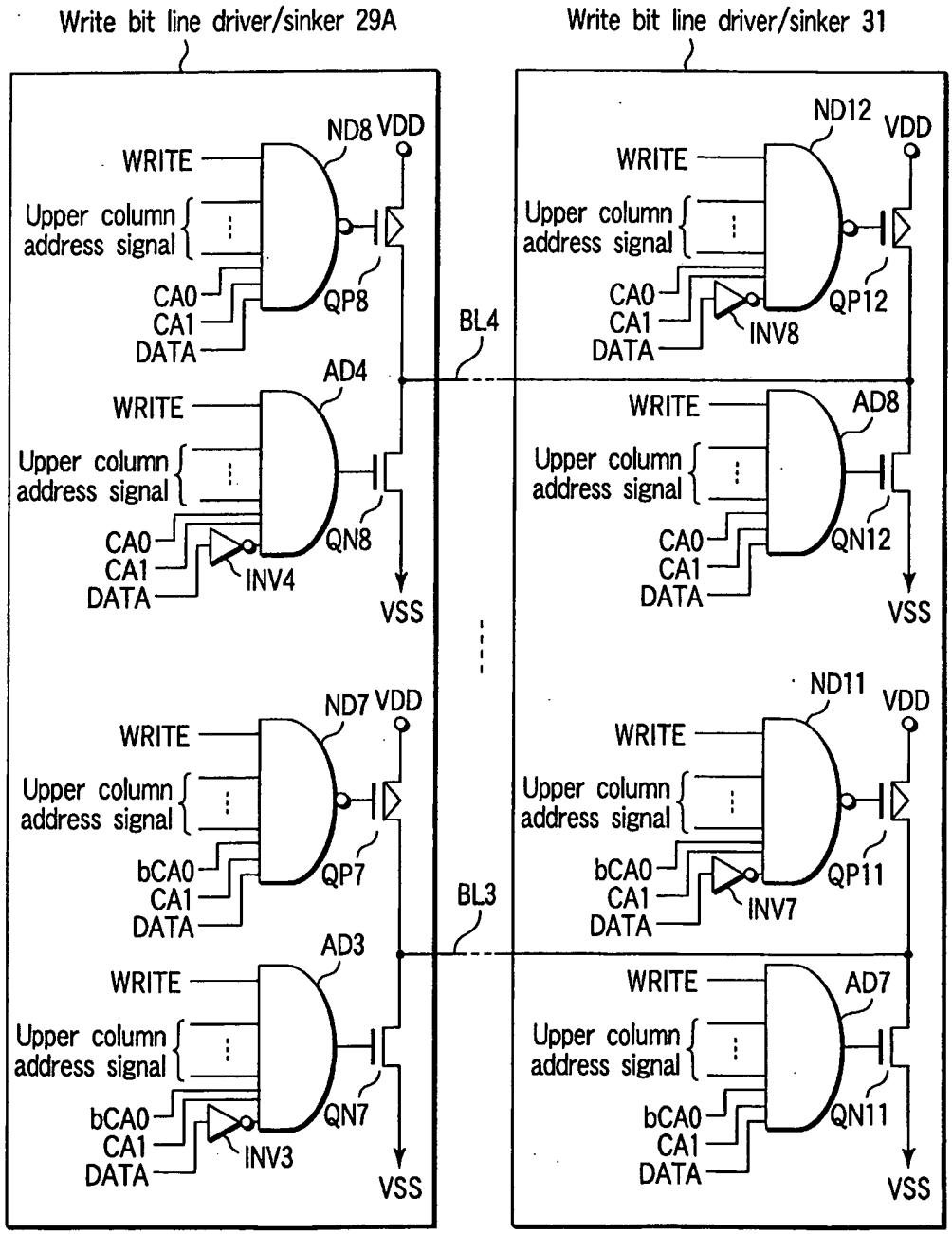
Write bit line driver/sinker 29A
Write bit line driver/sinker 31
ND8
VDD
WRITE
Upper column address signal
CA0
CA1
DATA
QP8
BL4
AD4
QN8
INV4
VSS
ND12
QP12
INV8
AD8
QN12
ND7
bCA0
QP7
BL3
AD3
QN7
INV3
ND11
QP11
INV7
AD7
QN11

FIG. 76

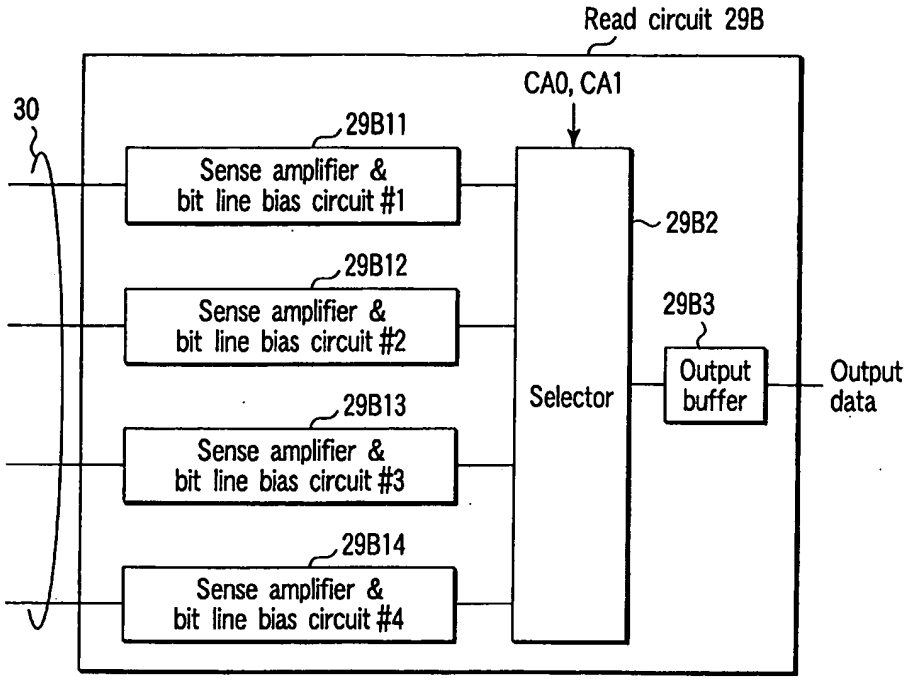
Read circuit 29B
CA0, CA1
30
29B11
Sense amplifier & bit line bias circuit #1
29B12
Sense amplifier & bit line bias circuit #2
29B13
Sense amplifier & bit line bias circuit #3
29B14
Sense amplifier & bit line bias circuit #4
Selector
29B2
29B3
Output buffer
Output data

FIG. 77

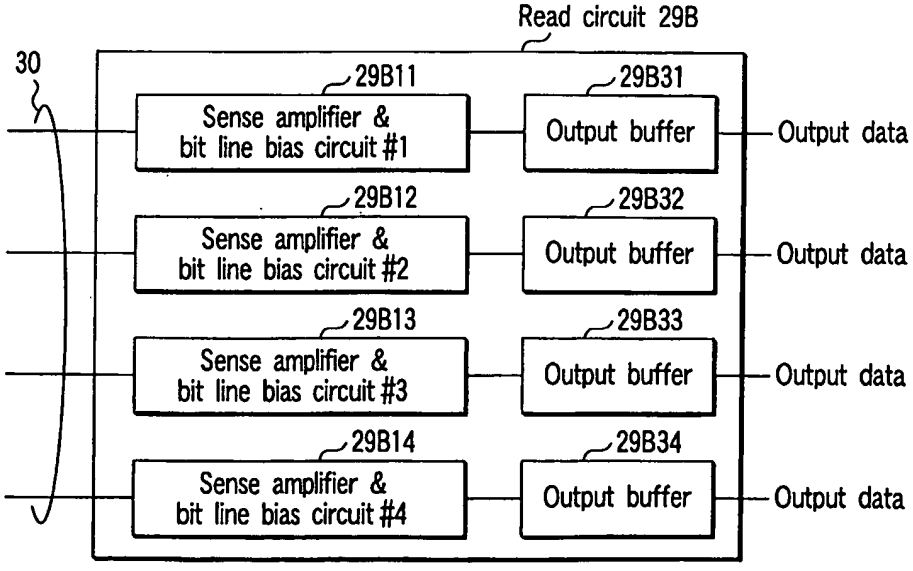
Read circuit 29B
30
29B11
Sense amplifier & bit line bias circuit #1
29B31
Output buffer
Output data
29B12
Sense amplifier & bit line bias circuit #2
29B32
Output buffer
Output data
29B13
Sense amplifier & bit line bias circuit #3
29B33
Output buffer
Output data
29B14
Sense amplifier & bit line bias circuit #4
29B34
Output buffer
Output data

FIG. 78

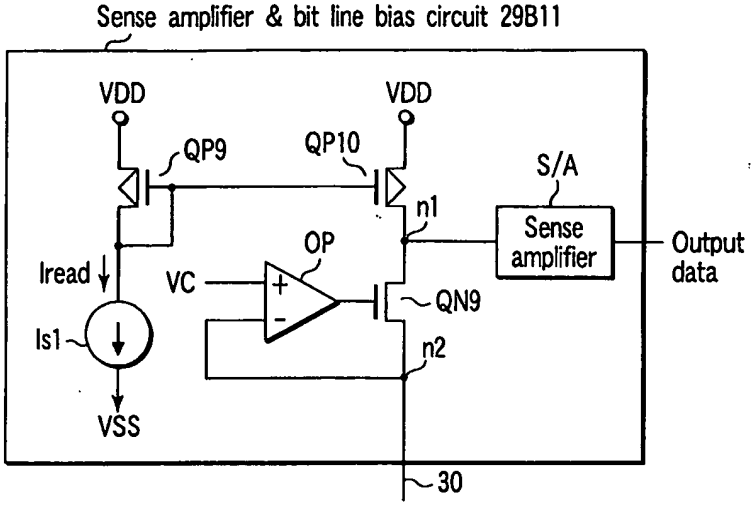

FIG. 79

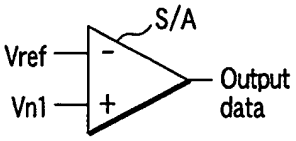

FIG. 80

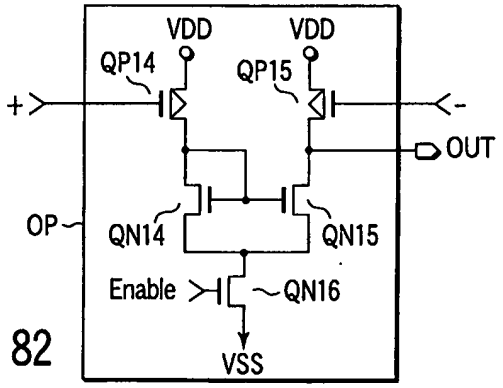

FIG. 82

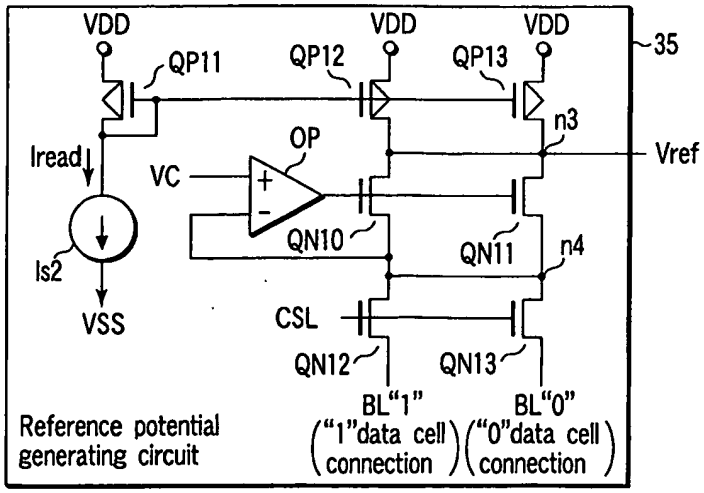

FIG. 81

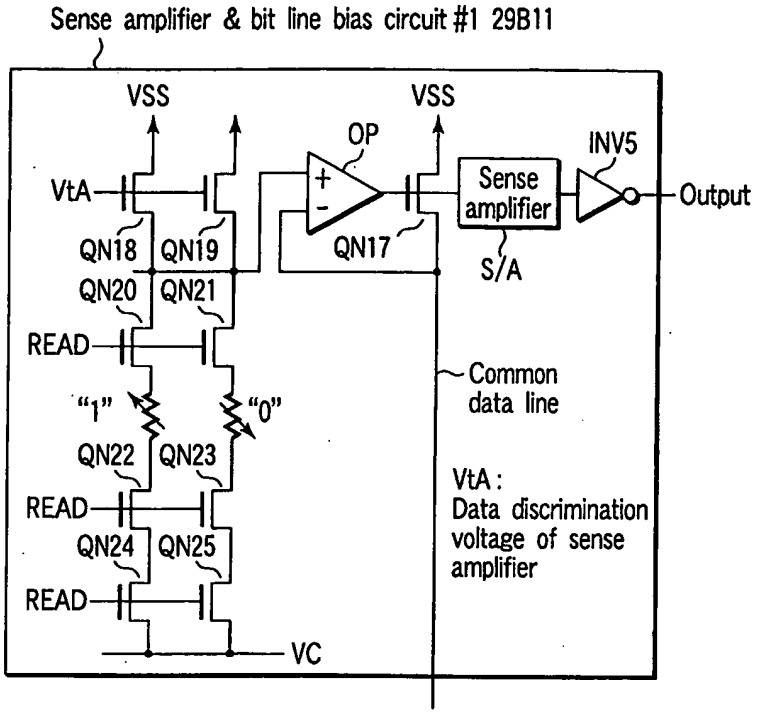
Sense amplifier & bit line bias circuit #1 29B11
VSS
VSS
OP
INV5
VtA
Sense amplifier
Output
QN18
QN19
QN17
S/A
QN20
QN21
READ
Common data line
"1"
"0"
QN22
QN23
READ
VtA:
Data discrimination voltage of sense amplifier
QN24
QN25
READ
VC

FIG. 83

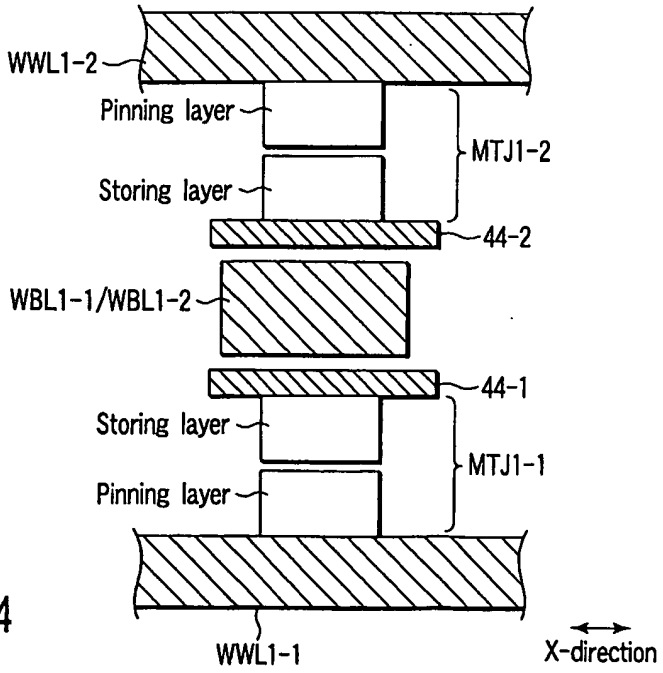
WWL1-2
Pinning layer
MTJ1-2
Storing layer
44-2
WBL1-1/WBL1-2
44-1
Storing layer
MTJ1-1
Pinning layer
WWL1-1
X-direction

FIG. 84

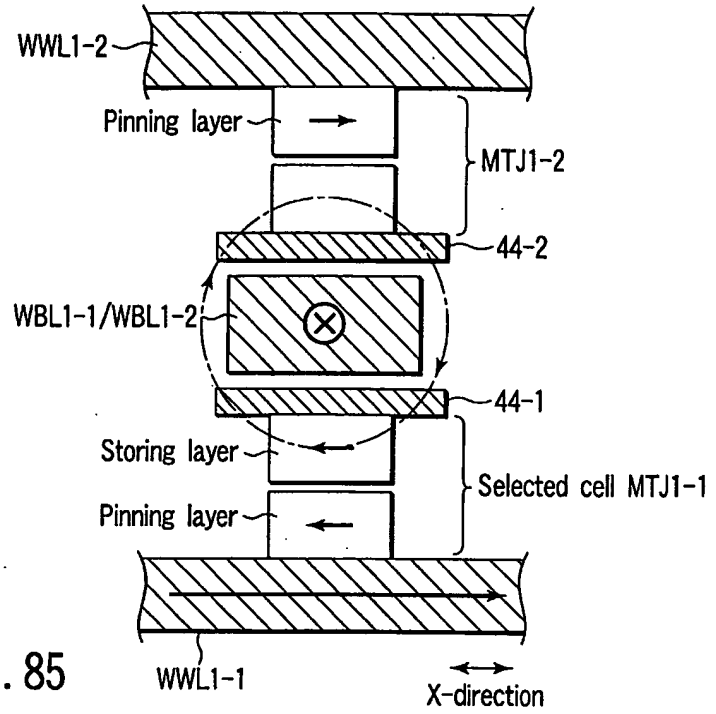
WWL1-2
Pinning layer
MTJ1-2
44-2
WBL1-1/WBL1-2
44-1
Storing layer
Selected cell MTJ1-1
Pinning layer
WWL1-1
X-direction

FIG. 85

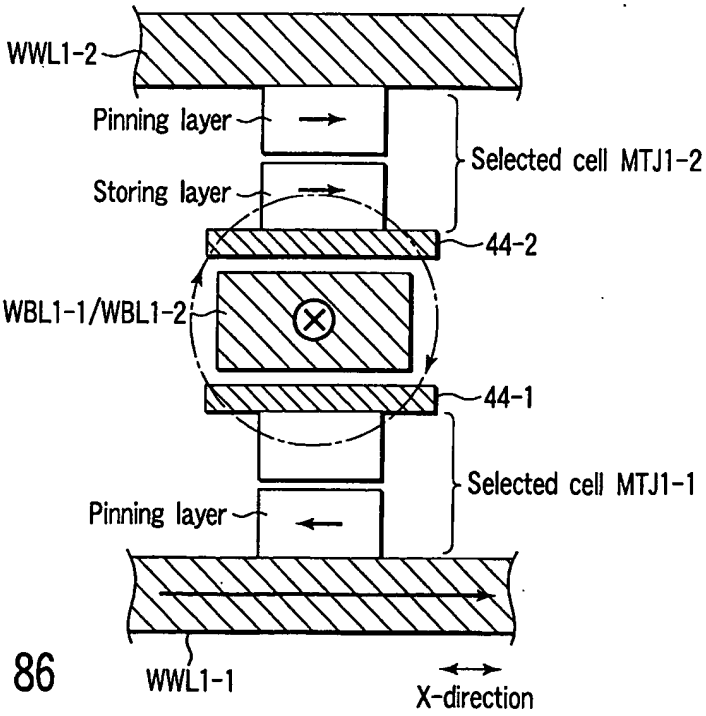
WWL1-2
Pinning layer
Selected cell MTJ1-2
Storing layer
44-2
WBL1-1/WBL1-2
44-1
Selected cell MTJ1-1
Pinning layer
WWL1-1
X-direction

FIG. 86

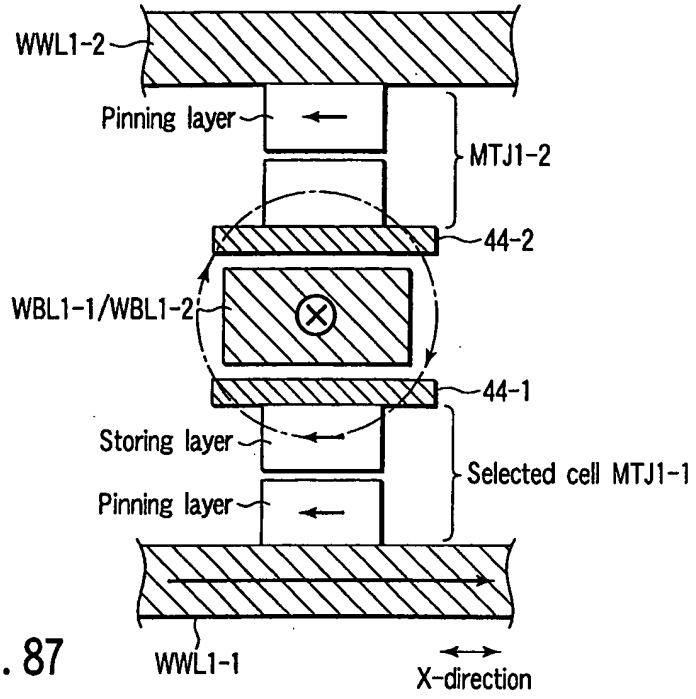
WWL1-2
Pinning layer
MTJ1-2
44-2
WBL1-1/WBL1-2
44-1
Storing layer
Selected cell MTJ1-1
Pinning layer
WWL1-1
X-direction

FIG. 87

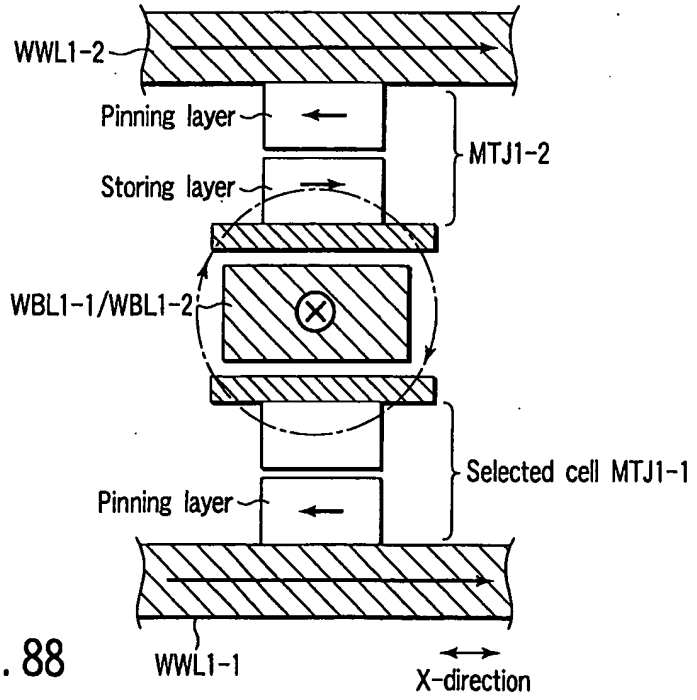
WWL1-2
Pinning layer
MTJ1-2
Storing layer
WBL1-1/WBL1-2
Selected cell MTJ1-1
Pinning layer
WWL1-1
X-direction

FIG. 88

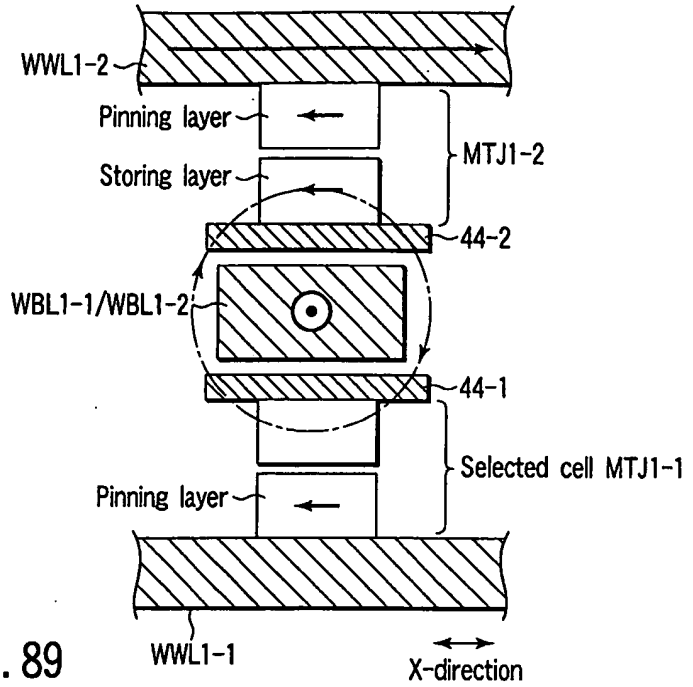
WWL1-2
Pinning layer
Storing layer
MTJ1-2
44-2
WBL1-1/WBL1-2
44-1
Selected cell MTJ1-1
Pinning layer
WWL1-1
X-direction

FIG. 89

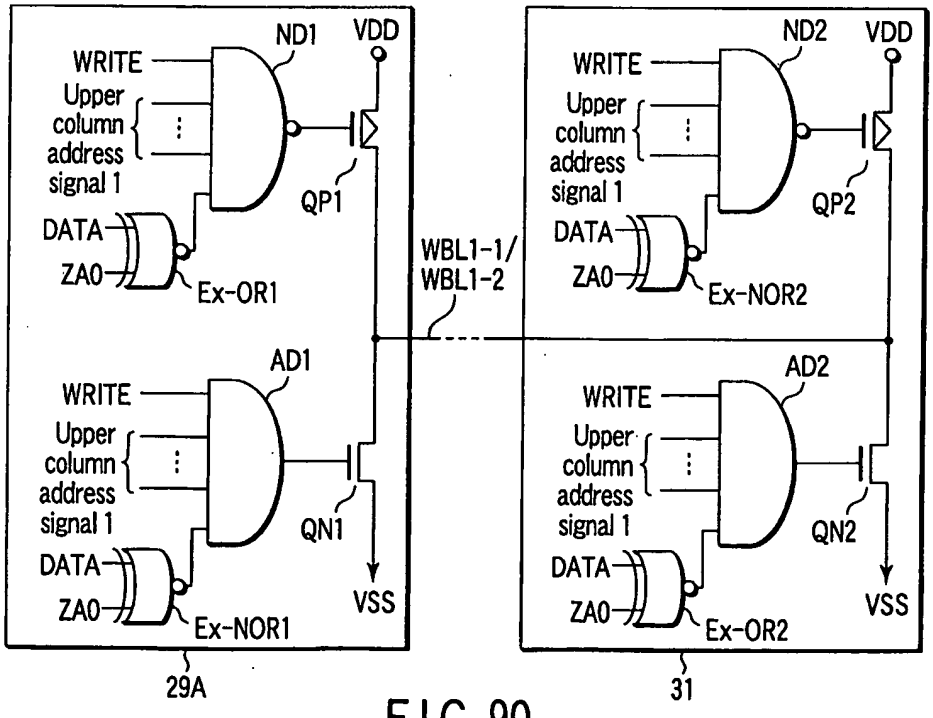
ND1
VDD
WRITE
Upper column address signal 1
DATA
ZA0
Ex-OR1
QP1
WBL1-1/ WBL1-2
ND2
VDD
WRITE
Upper column address signal 1
DATA
ZA0
Ex-NOR2
QP2
AD1
WRITE
Upper column address signal 1
DATA
ZA0
Ex-NOR1
QN1
VSS
29A
AD2
WRITE
Upper column address signal 1
DATA
ZA0
Ex-OR2
QN2
VSS
31

FIG. 90

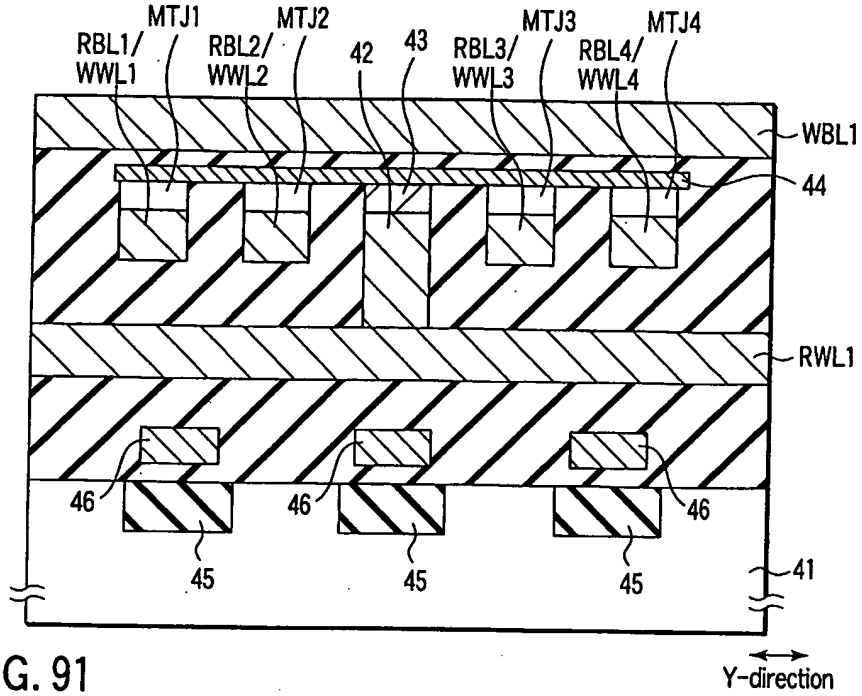

FIG. 91

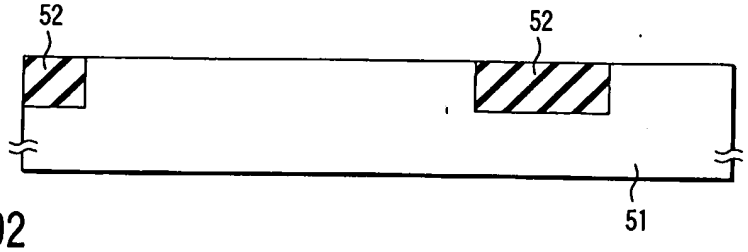

FIG. 92

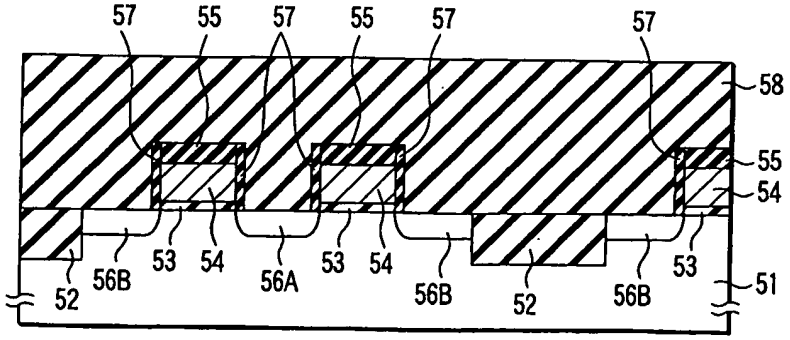

FIG. 93

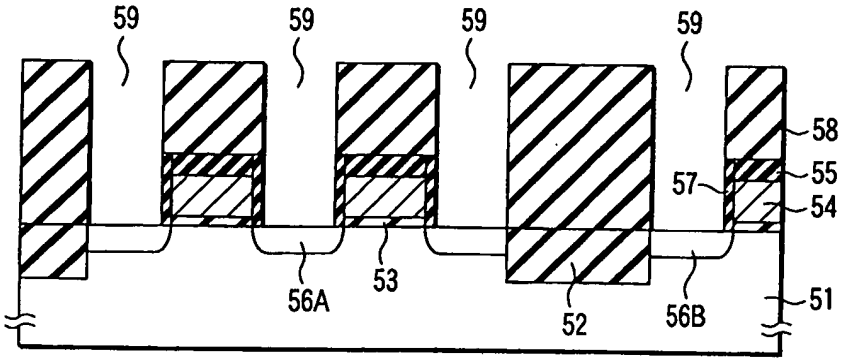

FIG. 94

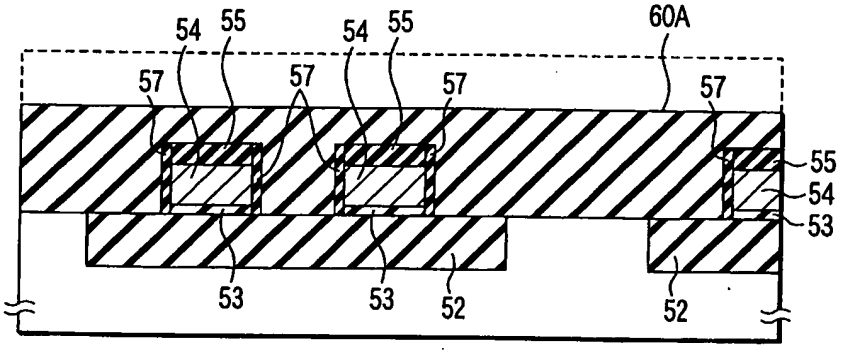

FIG. 95

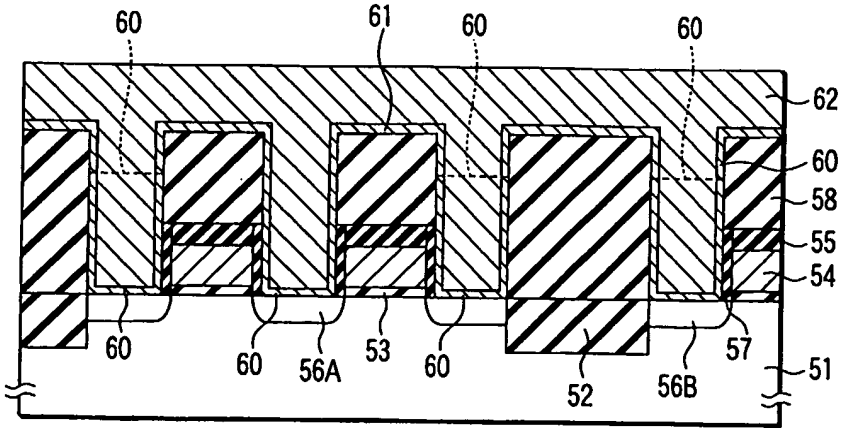

FIG. 96

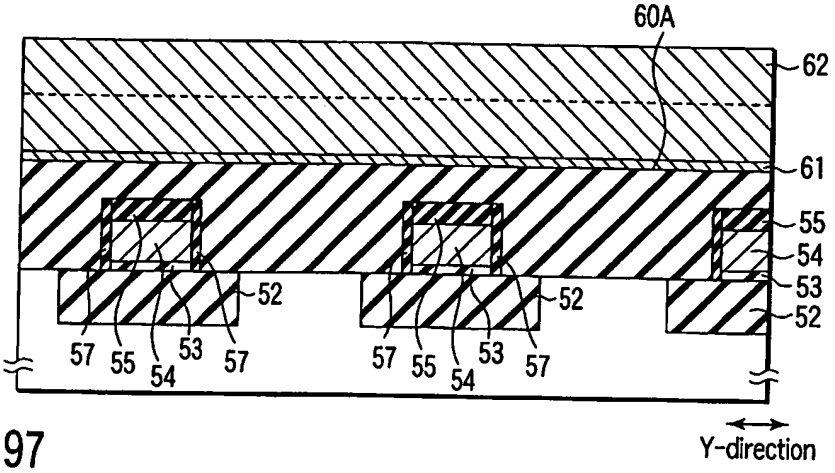

FIG. 97

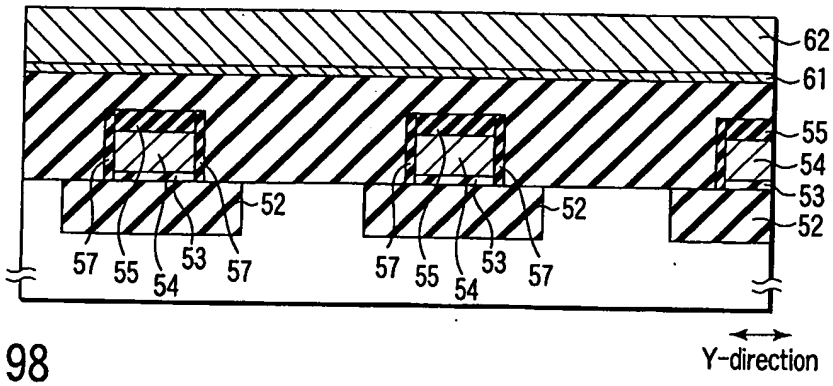

FIG. 98

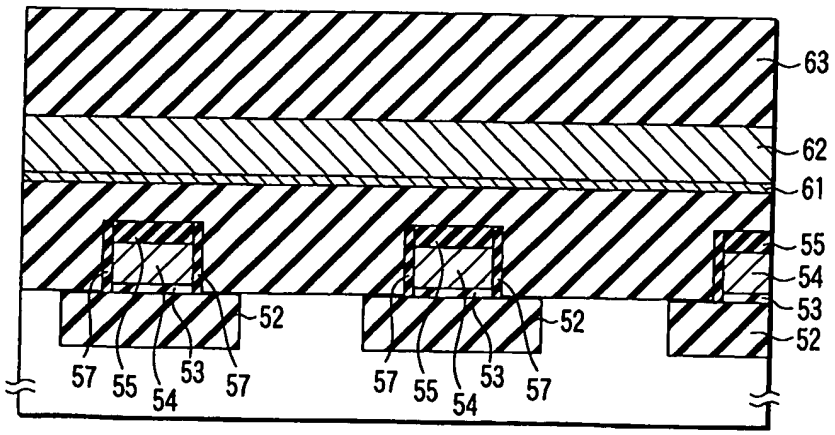

FIG. 99

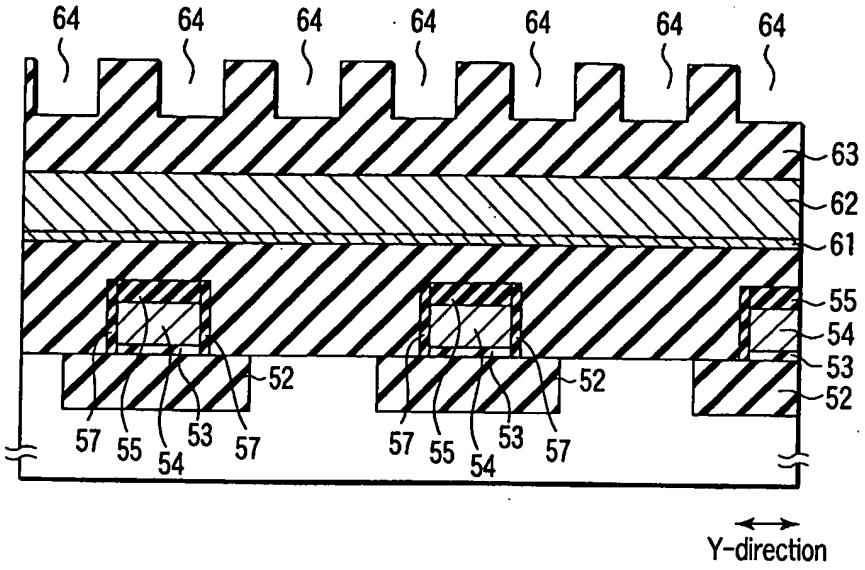

FIG. 100

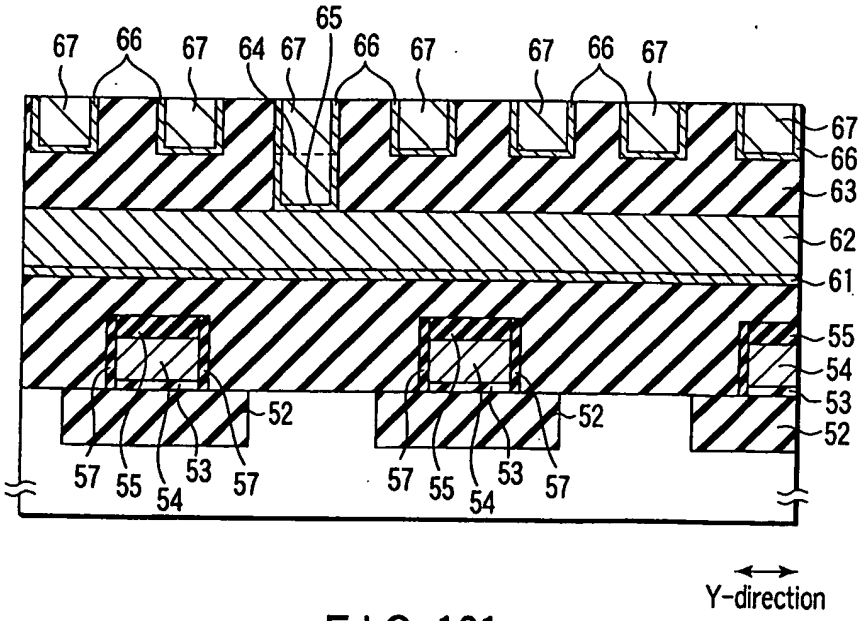

FIG. 101

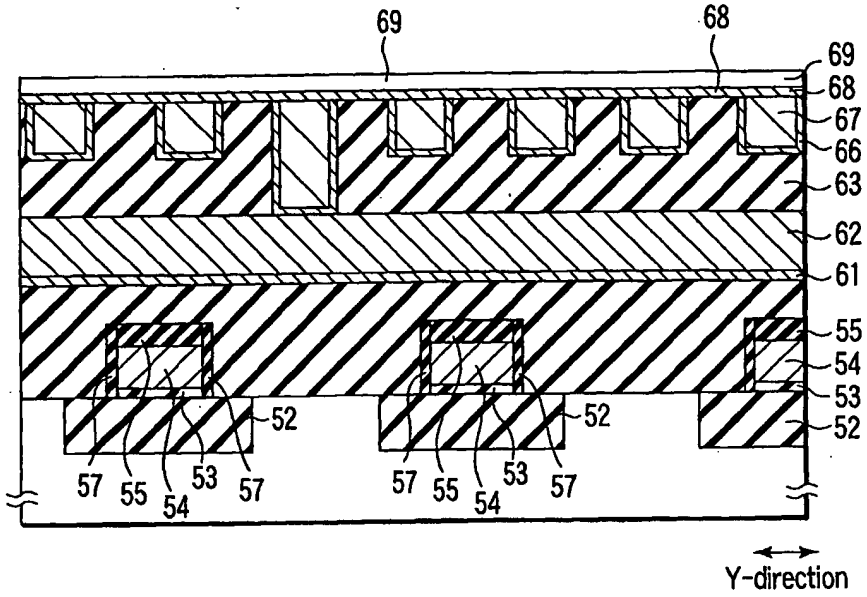

FIG. 102

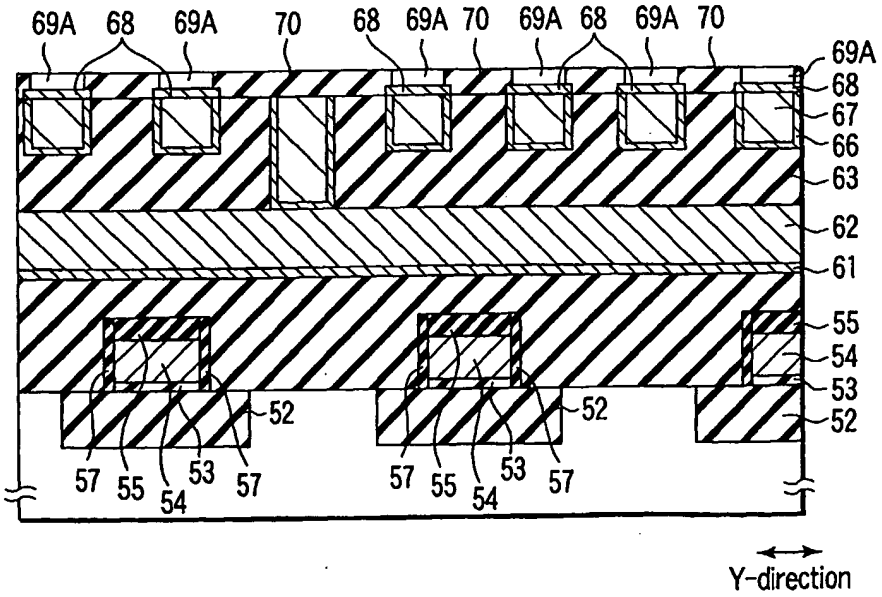

FIG. 103

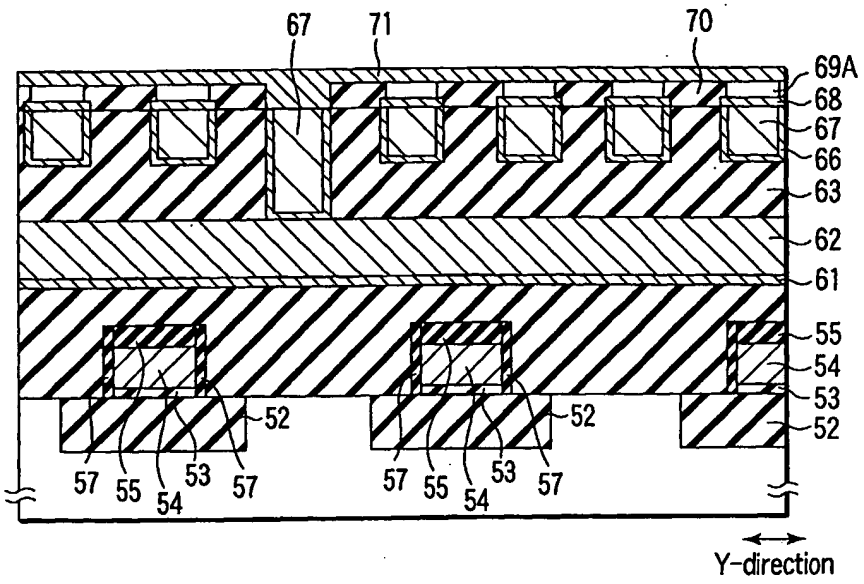

FIG. 104

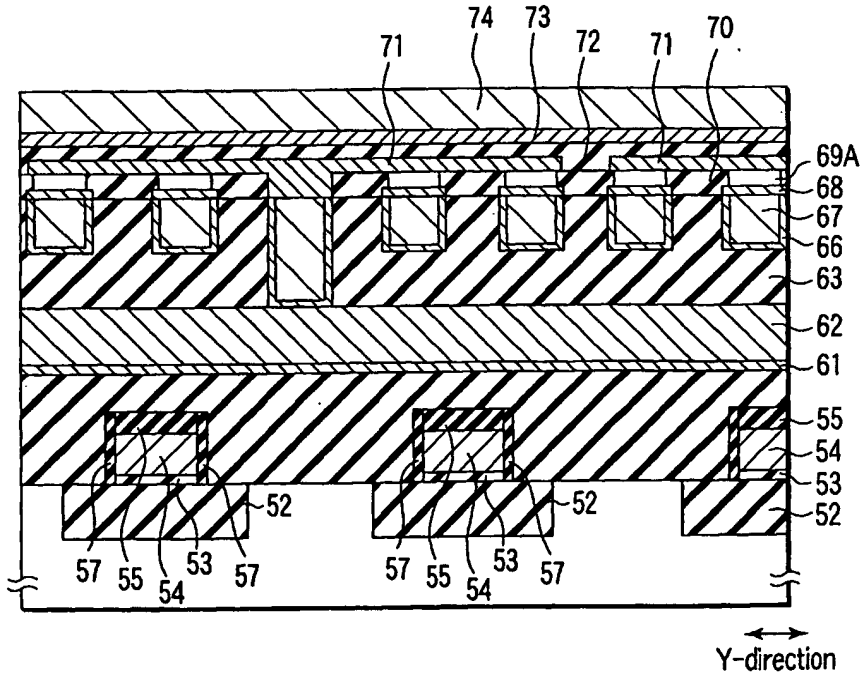

FIG. 105

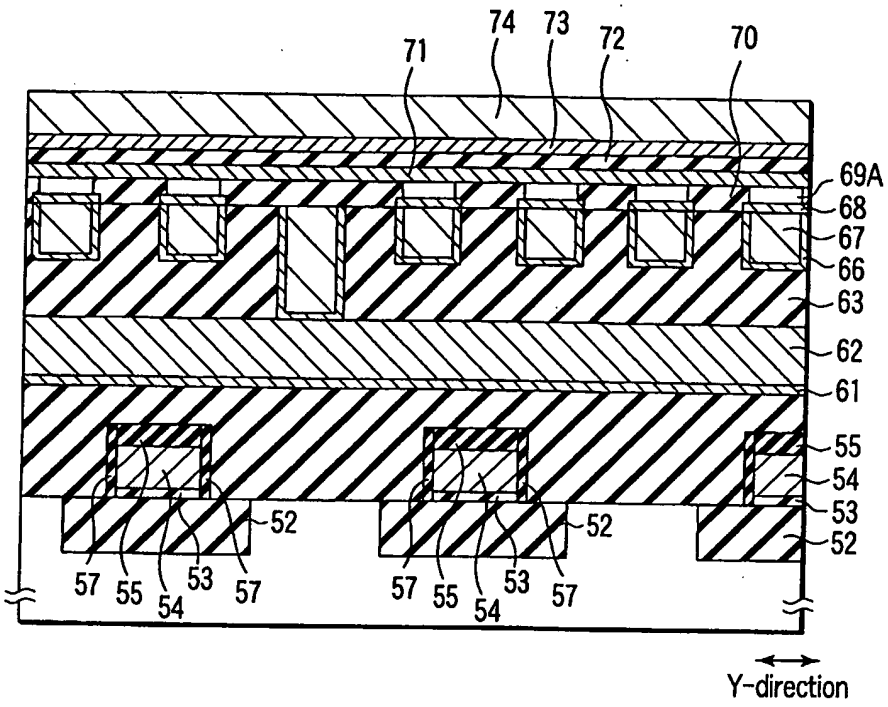

FIG. 106

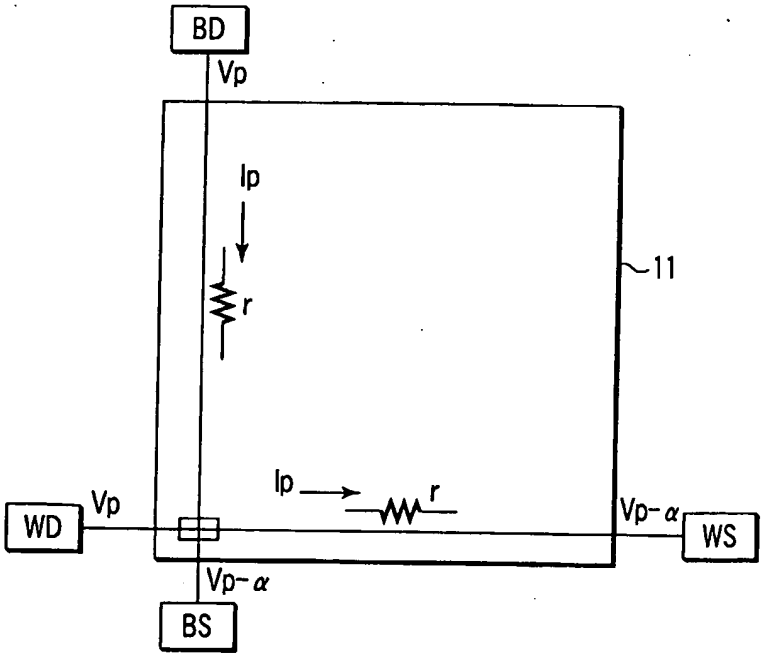

FIG. 107

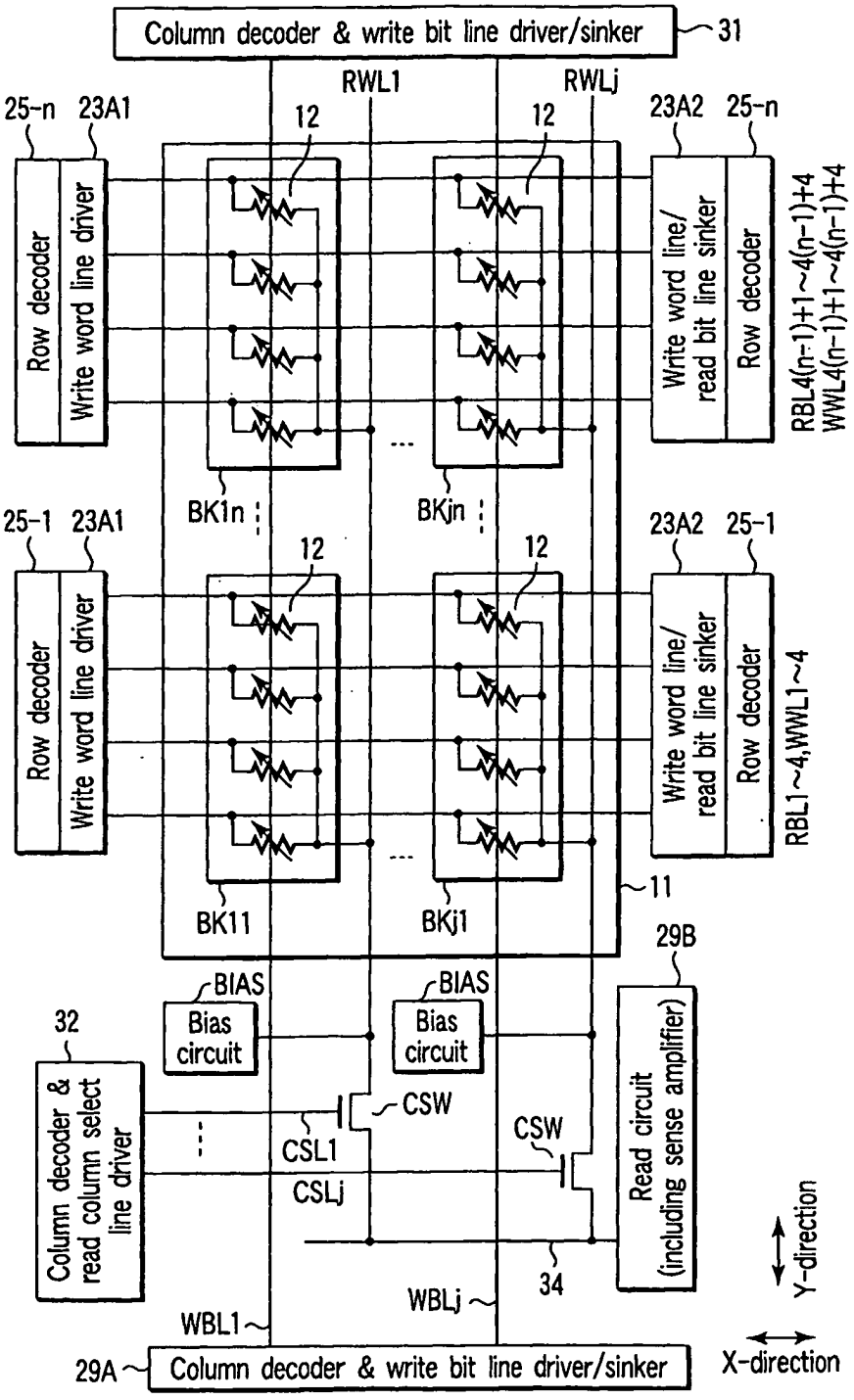
Column decoder & write bit line driver/sinker
31
RWL1
RWLj
25-n
23A1
12
23A2
25-n
Row decoder
Write word line driver
Write word line/ read bit line sinker
Row decoder
RBL4(n-1)+1~4(n-1)+4
WWL4(n-1)+1~4(n-1)+4
BK1n
BKjn
25-1
23A1
23A2
25-1
RBL1~4,WWL1~4
11
BK11
BKj1
29B
BIAS
Bias circuit
32
Column decoder & read column select line driver
CSW
CSL1
CSLj
Read circuit (including sense amplifier)
34
WBL1
WBLj
29A
Column decoder & write bit line driver/sinker
Y-direction
X-direction

FIG. 108

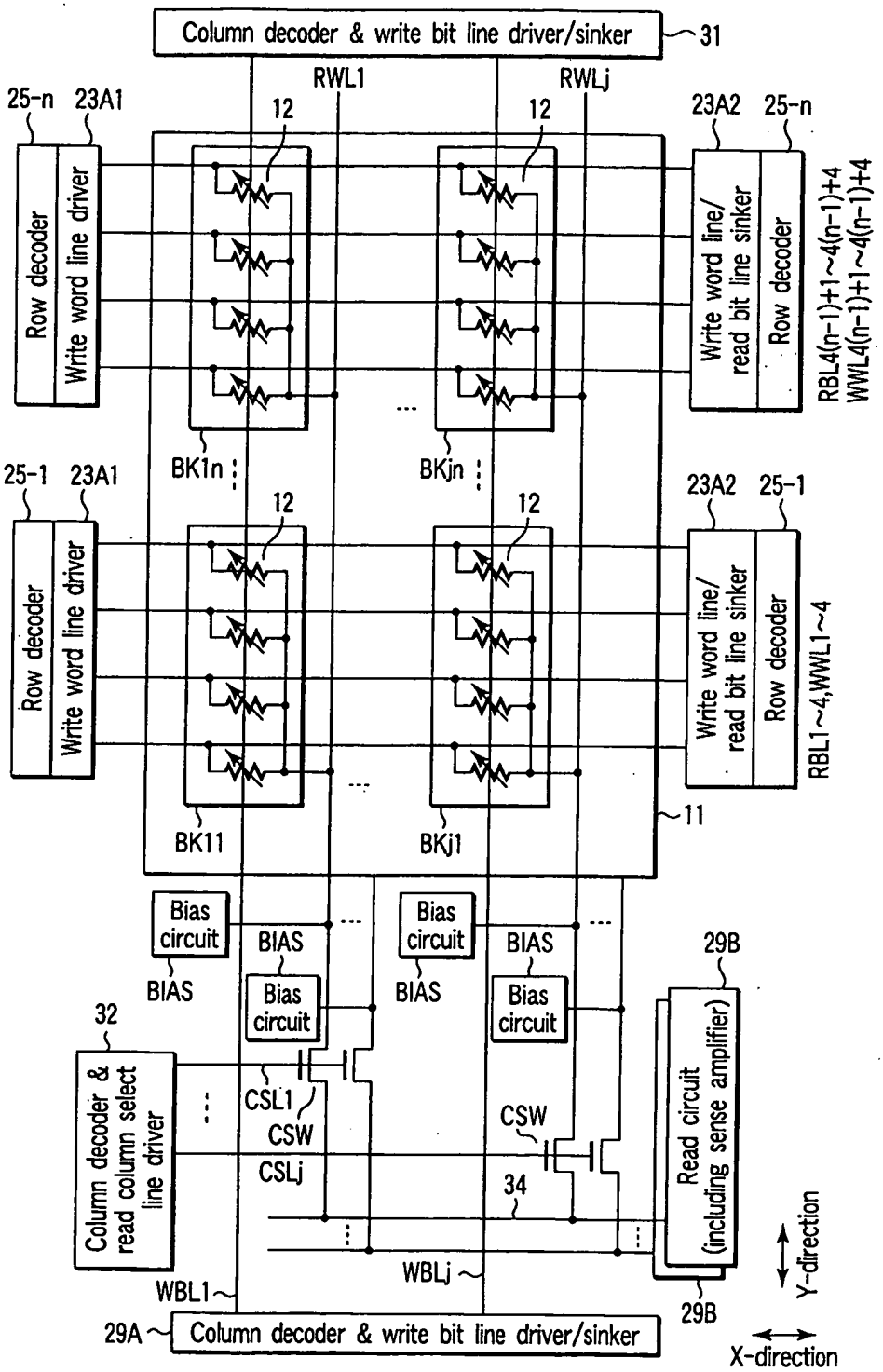
Column decoder & write bit line driver/sinker
31
RWL1
RWLj
12
25-n
23A1
Row decoder
Write word line driver
23A2
Write word line/ read bit line sinker
Row decoder
RBL4(n-1)+1~4(n-1)+4
WWL4(n-1)+1~4(n-1)+4
BK1n
BKjn
25-1
BK11
BKj1
11
RBL1~4,WWL1~4
Bias circuit
BIAS
29B
32
Column decoder & read column select line driver
CSL1
CSW
CSLj
34
Read circuit (including sense amplifier)
WBL1
WBLj
29A
Y-direction
X-direction

FIG. 109

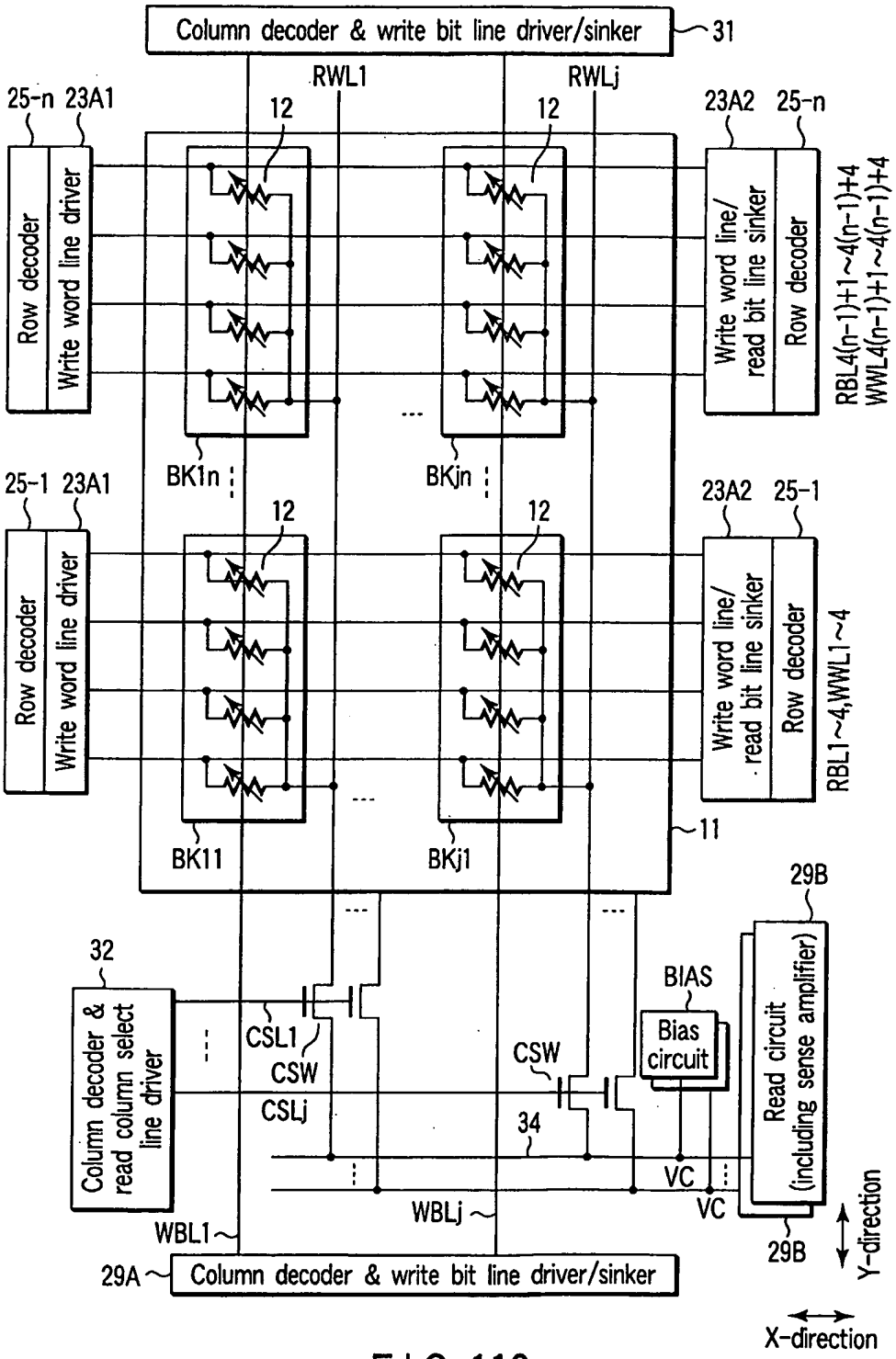
Column decoder & write bit line driver/sinker
31
RWL1
RWLj
25-n 23A1
12
23A2 25-n
Row decoder
Write word line driver
Write word line/ read bit line sinker
Row decoder
RBL4(n-1)+1~4(n-1)+4
WWL4(n-1)+1~4(n-1)+4
BK1n
BKjn
25-1 23A1
23A2 25-1
RBL1~4,WWL1~4
BK11
BKj1
11
29B
32
BIAS
Bias circuit
Read circuit (including sense amplifier)
Column decoder & read column select line driver
CSL1
CSW
CSLj
34
VC
WBL1
WBLj
29A
Column decoder & write bit line driver/sinker
Y-direction
X-direction

FIG. 110

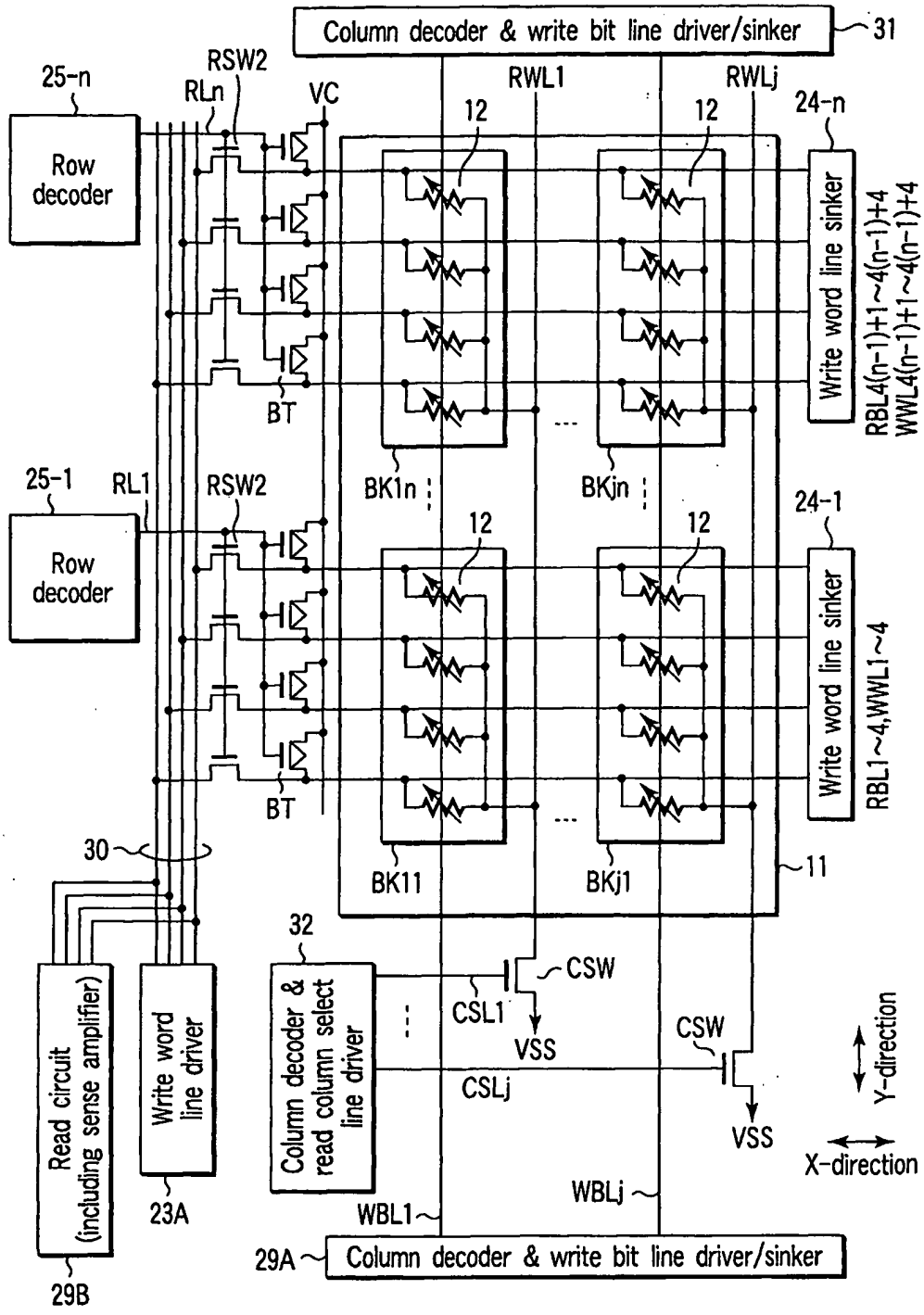
Column decoder & write bit line driver/sinker
31
25-n
RSW2
RLn
VC
RWL1
RWLj
12
24-n
Row decoder
Write word line sinker
RBL4(n-1)+1~4(n-1)+4
WWL4(n-1)+1~4(n-1)+4
BT
BK1n
BKjn
25-1
RL1
RSW2
24-1
Row decoder
Write word line sinker
RBL1~4,WWL1~4
BT
30
BK11
BKj1
11
32
CSW
CSL1
VSS
CSW
Column decoder & read column select line driver
CSLj
VSS
Y-direction
X-direction
Read circuit (including sense amplifier)
Write word line driver
23A
WBL1
WBLj
29A
Column decoder & write bit line driver/sinker
29B

FIG. 111

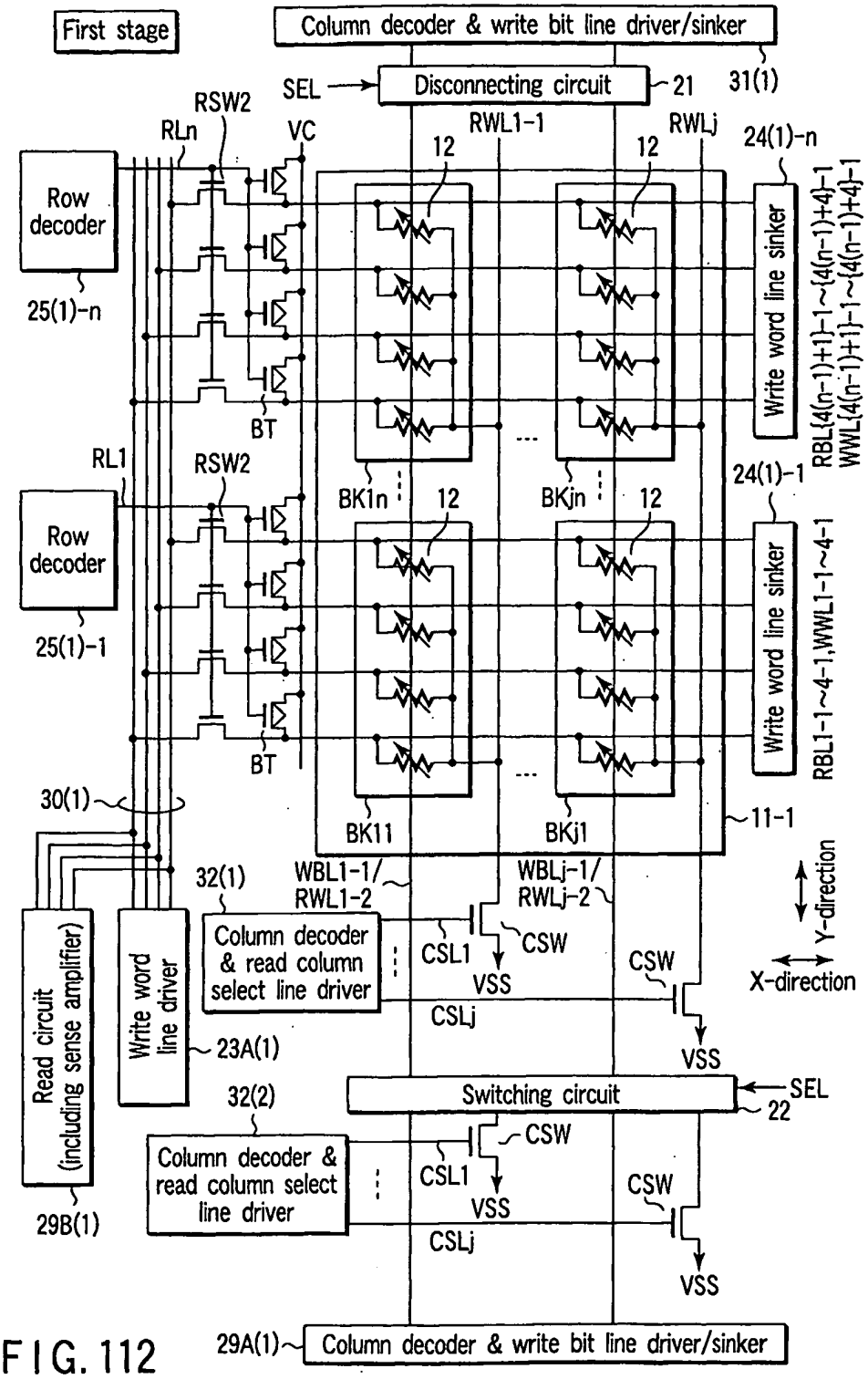
First stage
Column decoder & write bit line driver/sinker
31(1)
SEL
Disconnecting circuit
21
RSW2
RLn
VC
RWL1-1
RWLj
12
24(1)-n
Row decoder
25(1)-n
Write word line sinker
RBL{4(n-1)+1}-1~{4(n-1)+4}-1
WWL{4(n-1)+1}-1~{4(n-1)+4}-1
BT
RL1
RSW2
BK1n
BKjn
24(1)-1
Row decoder
25(1)-1
Write word line sinker
RBL1-1~4-1,WWL1-1~4-1
BT
30(1)
BK11
BKj1
11-1
32(1)
WBL1-1/
RWL1-2
WBLj-1/
RWLj-2
Y-direction
X-direction
Read circuit (including sense amplifier)
Write word line driver
Column decoder & read column select line driver
CSL1
CSW
VSS
CSLj
23A(1)
32(2)
Switching circuit
SEL
22
Column decoder & read column select line driver
29B(1)
29A(1)
Column decoder & write bit line driver/sinker

FIG. 112

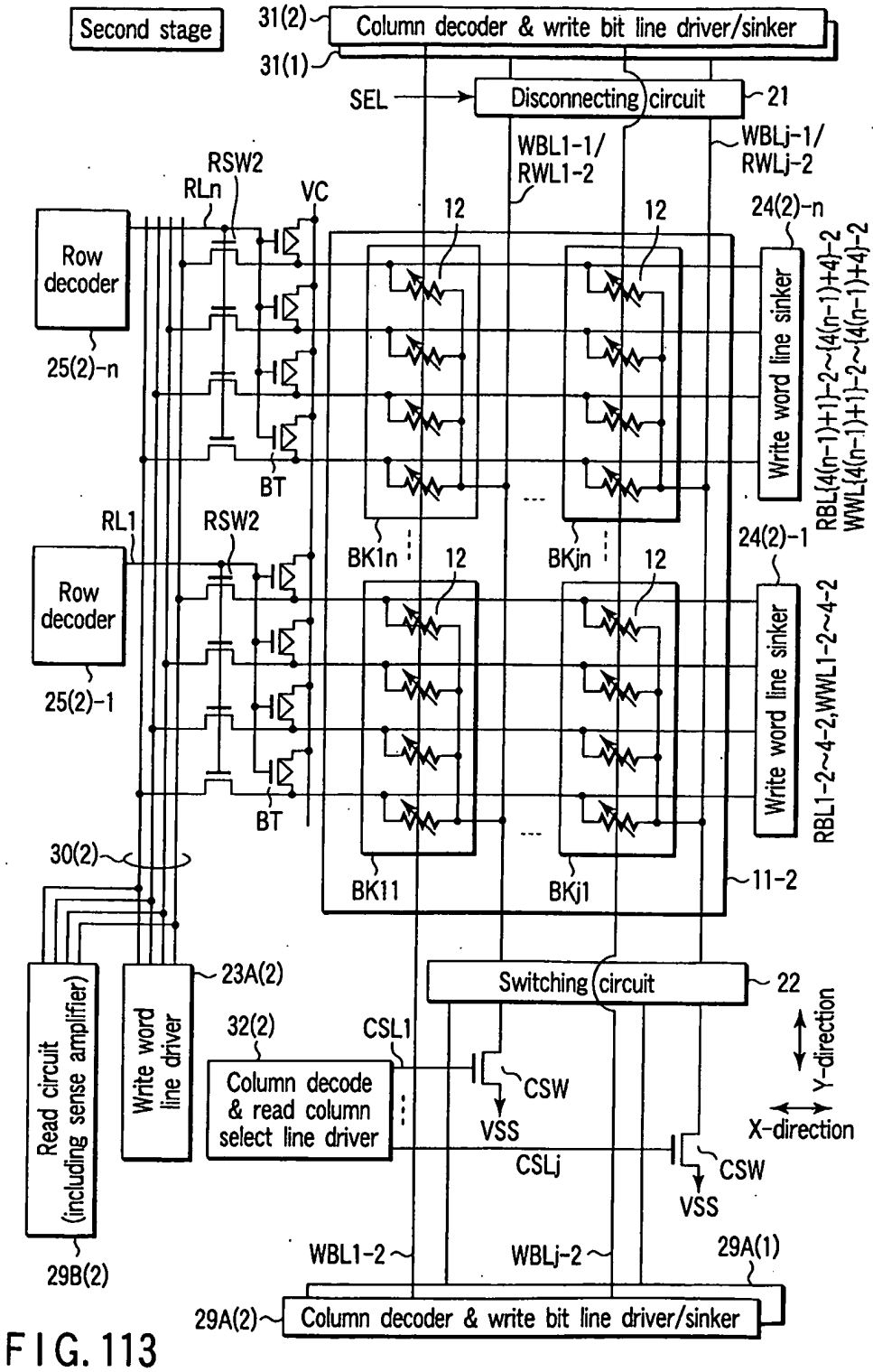
Second stage
31(2)
Column decoder & write bit line driver/sinker
31(1)
SEL
Disconnecting circuit
21
WBL1-1/
RWL1-2
WBLj-1/
RWLj-2
RSW2
RLn
VC
12
12
24(2)-n
Row
decoder
25(2)-n
Write word line sinker
RBL{4(n-1)+1}-2~{4(n-1)+4}-2
WWL{4(n-1)+1}-2~{4(n-1)+4}-2
BT
RL1
RSW2
BK1n
12
BKjn
12
24(2)-1
Row
decoder
25(2)-1
Write word line sinker
RBL1-2~4-2,WWL1-2~4-2
BT
30(2)
BK11
BKj1
11-2
Switching circuit
22
23A(2)
32(2)
CSL1
Write word
line driver
Column decode
& read column
select line driver
CSW
VSS
CSLj
CSW
VSS
Y-direction
X-direction
Read circuit
(including sense amplifier)
29B(2)
WBL1-2
WBLj-2
29A(1)
29A(2)
Column decoder & write bit line driver/sinker

FIG. 113

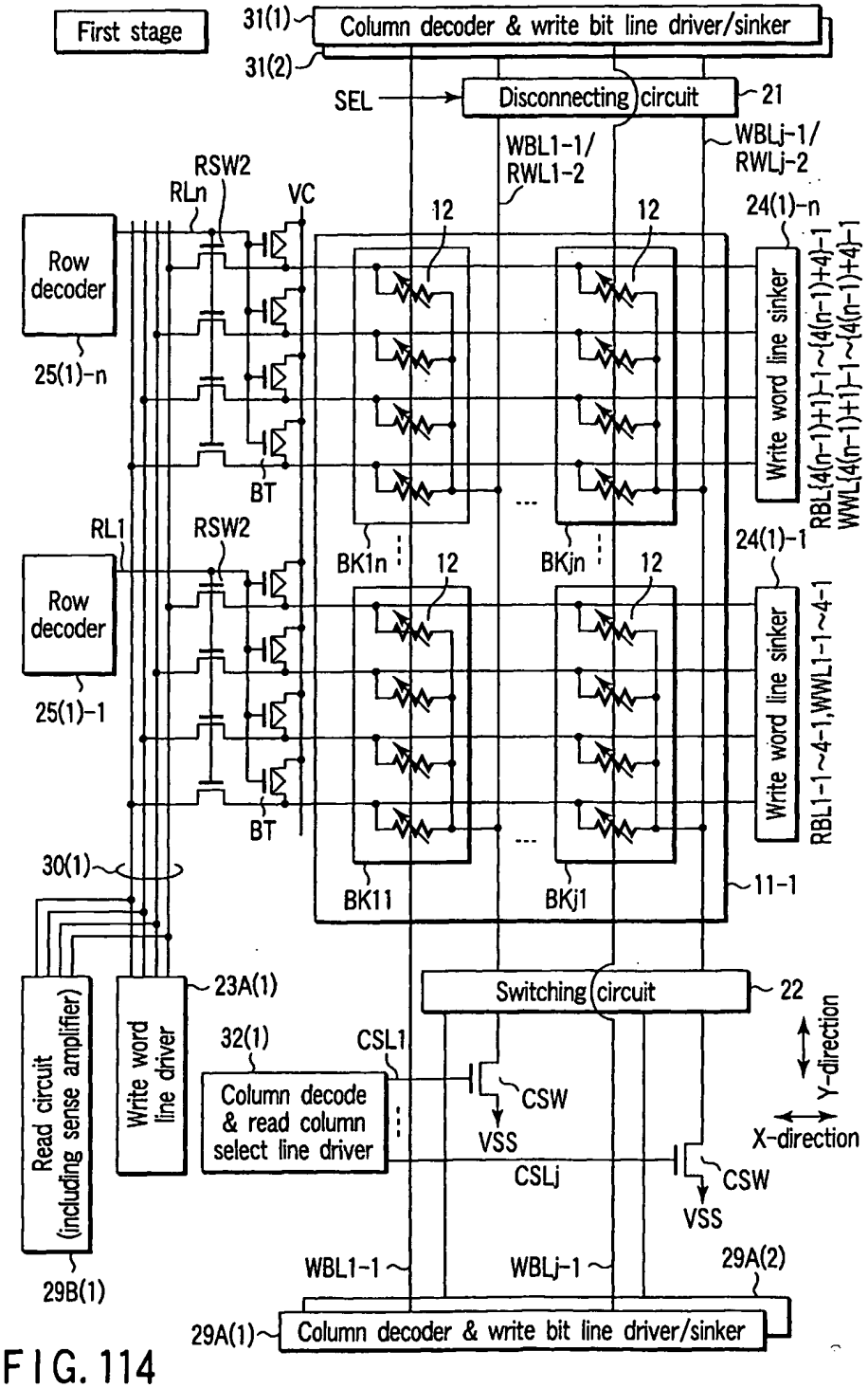
First stage
31(1)
Column decoder & write bit line driver/sinker
31(2)
SEL
Disconnecting circuit
21
WBL1-1/
RWL1-2
WBLj-1/
RWLj-2
RSW2
RLn
VC
12
12
24(1)-n
Row decoder
25(1)-n
Write word line sinker
RBL{4(n-1)+1}-1~{4(n-1)+4}-1
WWL{4(n-1)+1}-1~{4(n-1)+4}-1
BT
RL1
RSW2
BK1n
12
BKjn
12
24(1)-1
Row decoder
25(1)-1
Write word line sinker
RBL1-1~4-1,WWL1-1~4-1
BT
30(1)
BK11
BKj1
11-1
Read circuit (including sense amplifier)
Write word line driver
23A(1)
Switching circuit
22
32(1)
CSL1
Column decode & read column select line driver
CSW
VSS
CSLj
CSW
VSS
Y-direction
X-direction
29B(1)
WBL1-1
WBLj-1
29A(2)
29A(1)
Column decoder & write bit line driver/sinker

FIG. 114

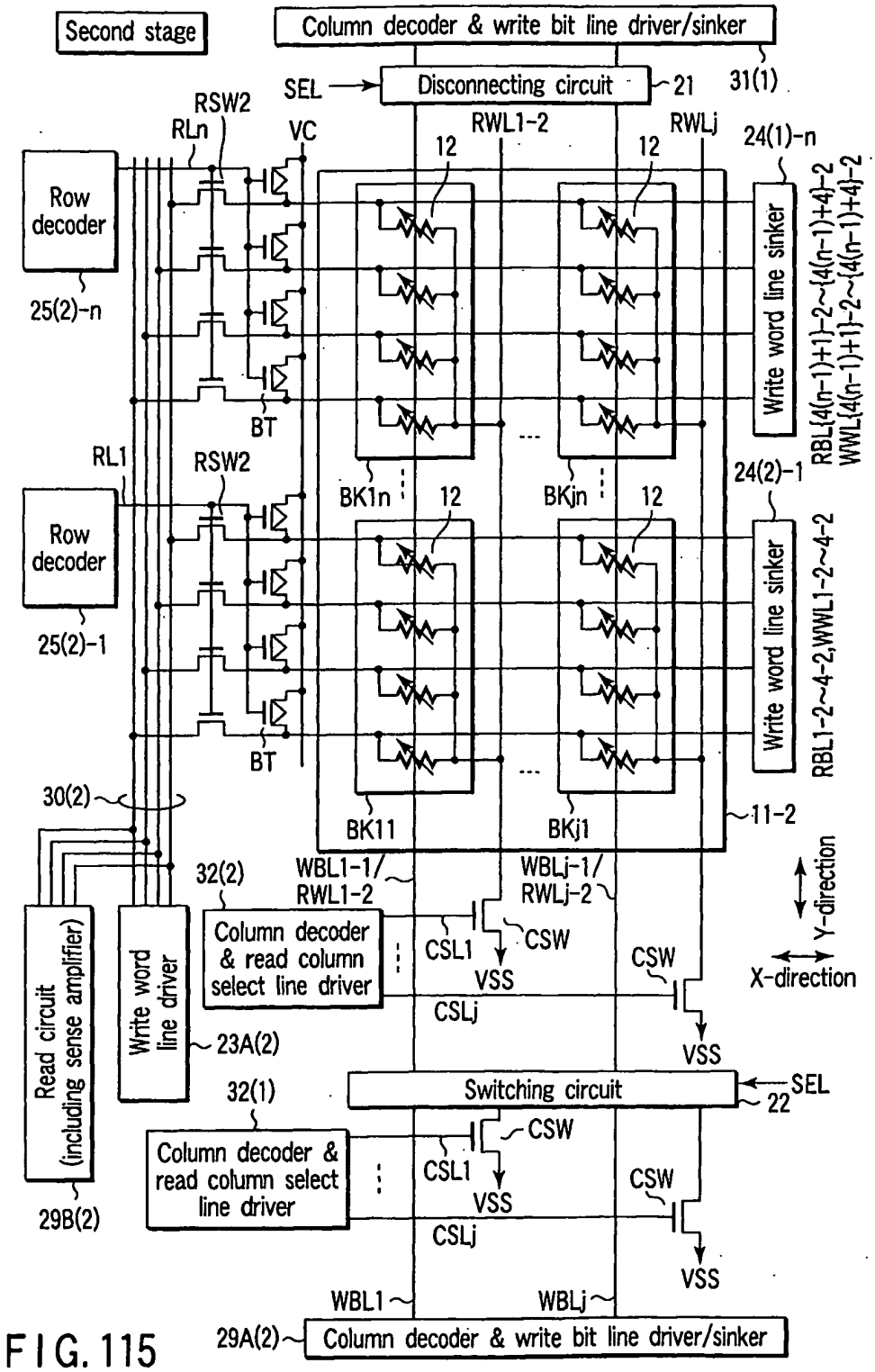
Second stage
Column decoder & write bit line driver/sinker
31(1)
SEL
Disconnecting circuit
21
RSW2
RLn
VC
RWL1-2
RWLj
12
24(1)-n
Row decoder
25(2)-n
BT
RL1
RSW2
BK1n
BKjn
24(2)-1
Row decoder
25(2)-1
Write word line sinker
RBL{4(n-1)+1}-2~{4(n-1)+4}-2
WWL{4(n-1)+1}-2~{4(n-1)+4}-2
RBL1-2~4-2,WWL1-2~4-2
30(2)
BK11
BKj1
11-2
32(2)
WBL1-1/
RWL1-2
WBLj-1/
RWLj-2
Y-direction
X-direction
Column decoder & read column select line driver
CSL1
CSW
VSS
CSLj
Read circuit (including sense amplifier)
Write word line driver
23A(2)
32(1)
Switching circuit
22
SEL
Column decoder & read column select line driver
29B(2)
WBL1
WBLj
29A(2)
Column decoder & write bit line driver/sinker

FIG. 115

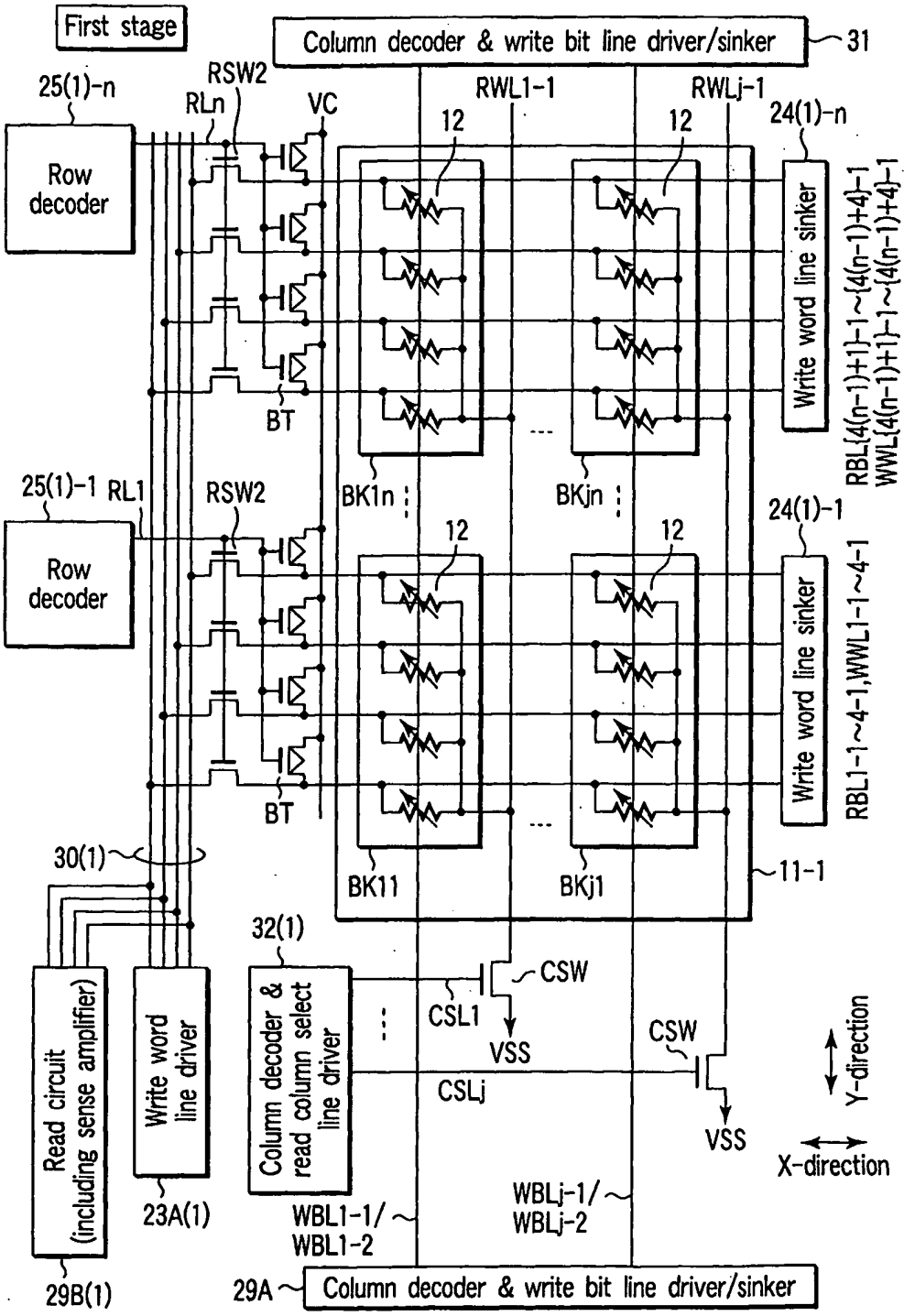
First stage
Column decoder & write bit line driver/sinker
31
25(1)-n
RSW2
RLn
VC
RWL1-1
RWLj-1
12
24(1)-n
Row decoder
Write word line sinker
BT
BK1n
BKjn
RBL{4(n-1)+1}-1~{4(n-1)+4}-1
WWL{4(n-1)+1}-1~{4(n-1)+4}-1
25(1)-1
RL1
RSW2
24(1)-1
Row decoder
Write word line sinker
RBL1-1~4-1,WWL1-1~4-1
BK11
BKj1
11-1
30(1)
32(1)
CSW
CSL1
VSS
CSLj
Y-direction
X-direction
Read circuit (including sense amplifier)
Write word line driver
Column decoder & read column select line driver
23A(1)
WBL1-1/ WBL1-2
WBLj-1/ WBLj-2
29B(1)
29A
Column decoder & write bit line driver/sinker

FIG. 116

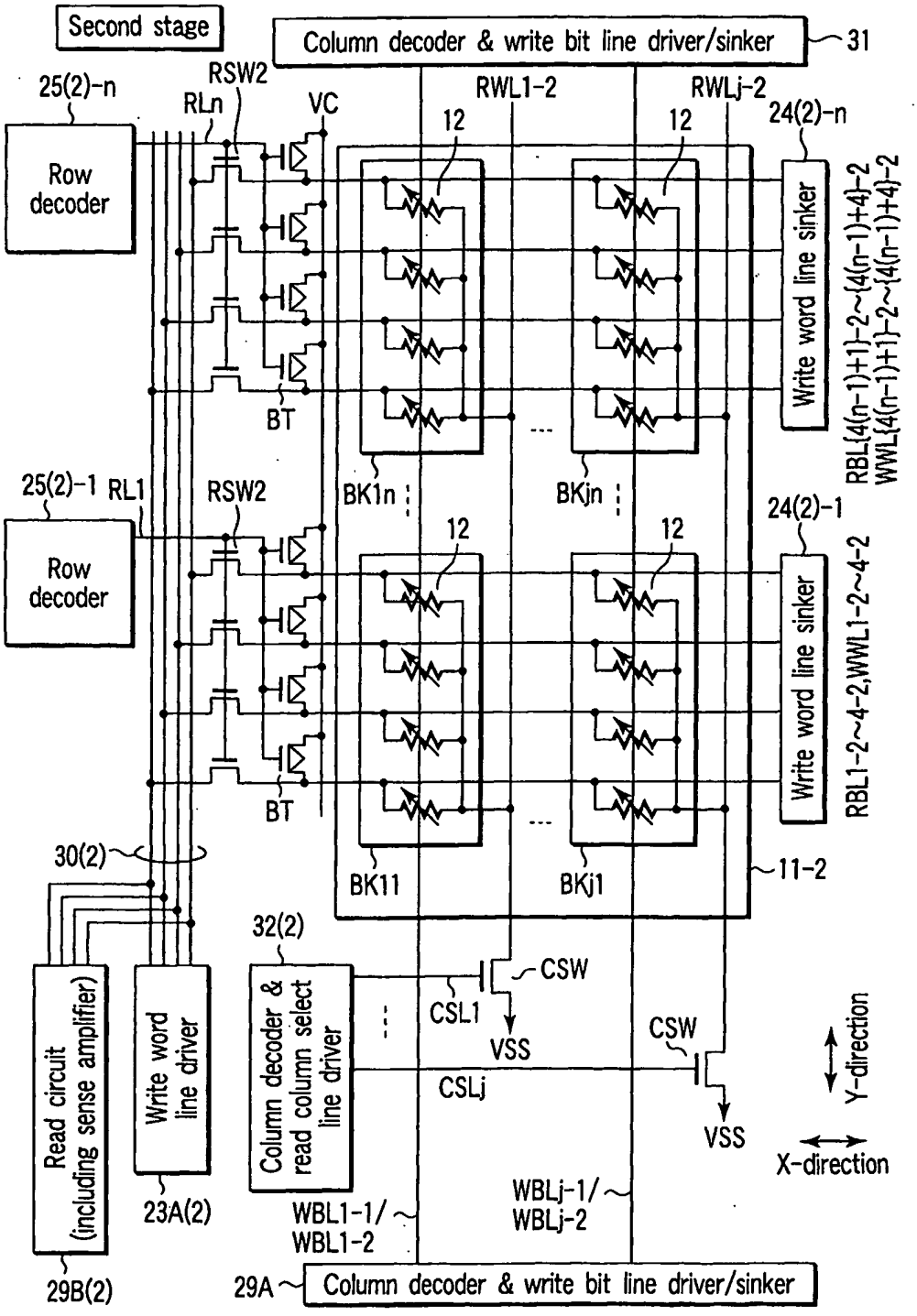
Second stage
Column decoder & write bit line driver/sinker
31
25(2)-n
RSW2
RLn
VC
RWL1-2
RWLj-2
12
24(2)-n
Row decoder
Write word line sinker
RBL{4(n-1)+1}-2~{4(n-1)+4}-2
WWL{4(n-1)+1}-2~{4(n-1)+4}-2
BT
BK1n
BKjn
25(2)-1
RL1
RSW2
24(2)-1
Row decoder
Write word line sinker
RBL1-2~4-2,WWL1-2~4-2
BT
30(2)
BK11
BKj1
11-2
32(2)
CSW
CSL1
VSS
CSW
CSLj
VSS
Y-direction
X-direction
Read circuit (including sense amplifier)
Write word line driver
Column decoder & read column select line driver
23A(2)
WBL1-1/ WBL1-2
WBLj-1/ WBLj-2
29B(2)
29A
Column decoder & write bit line driver/sinker

FIG. 117

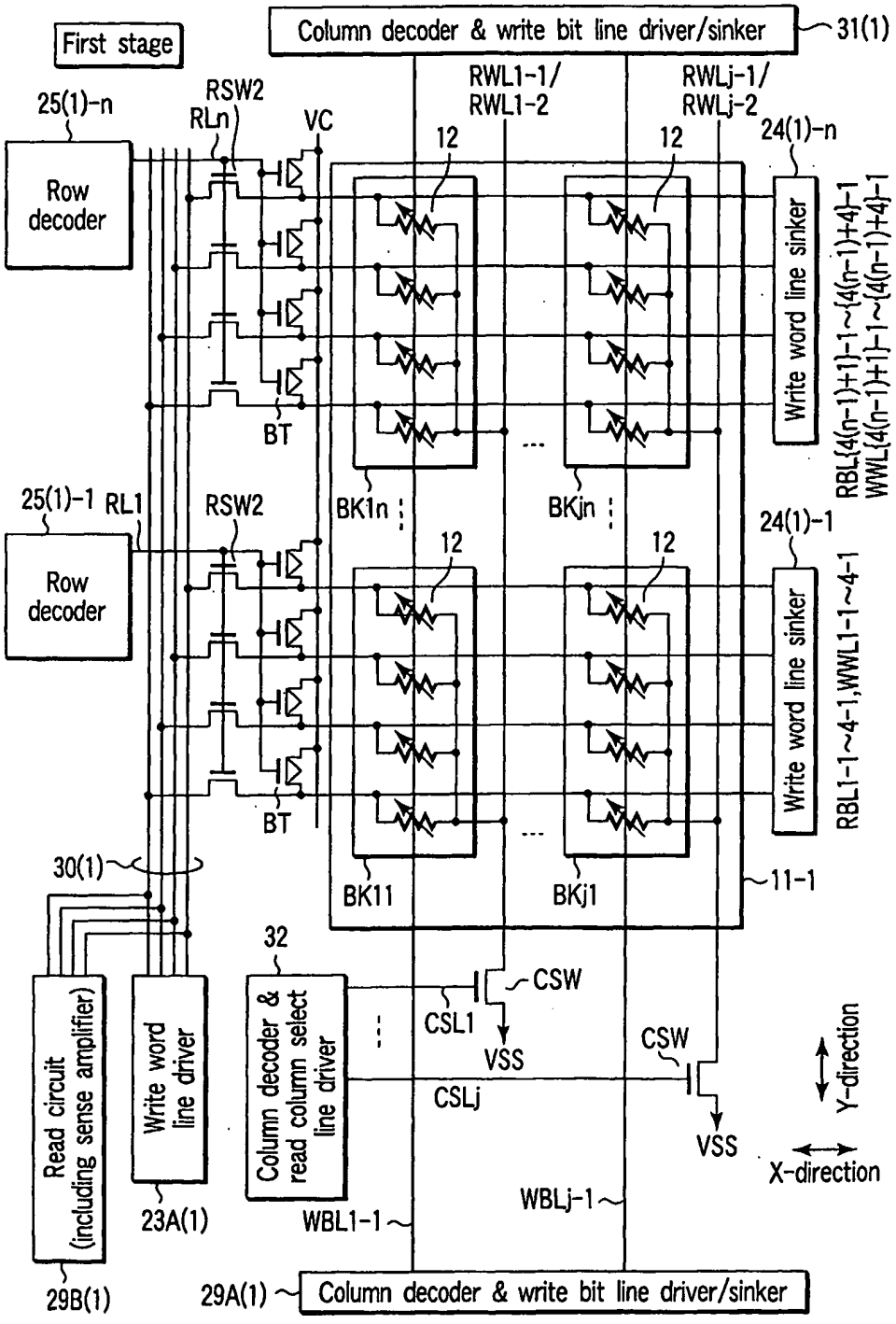
First stage
Column decoder & write bit line driver/sinker
31(1)
25(1)-n
RSW2
RLn
VC
RWL1-1/
RWL1-2
RWLj-1/
RWLj-2
12
24(1)-n
Row decoder
Write word line sinker
RBL{4(n-1)+1}-1~{4(n-1)+4}-1
WWL{4(n-1)+1}-1~{4(n-1)+4}-1
BT
25(1)-1
RL1
RSW2
BK1n
BKjn
24(1)-1
Row decoder
Write word line sinker
RBL1-1~4-1,WWL1-1~4-1
BT
30(1)
BK11
BKj1
11-1
32
CSW
CSL1
VSS
CSW
CSLj
VSS
Y-direction
X-direction
Read circuit (including sense amplifier)
Write word line driver
Column decoder & read column select line driver
23A(1)
WBL1-1
WBLj-1
29B(1)
29A(1)
Column decoder & write bit line driver/sinker

FIG. 118

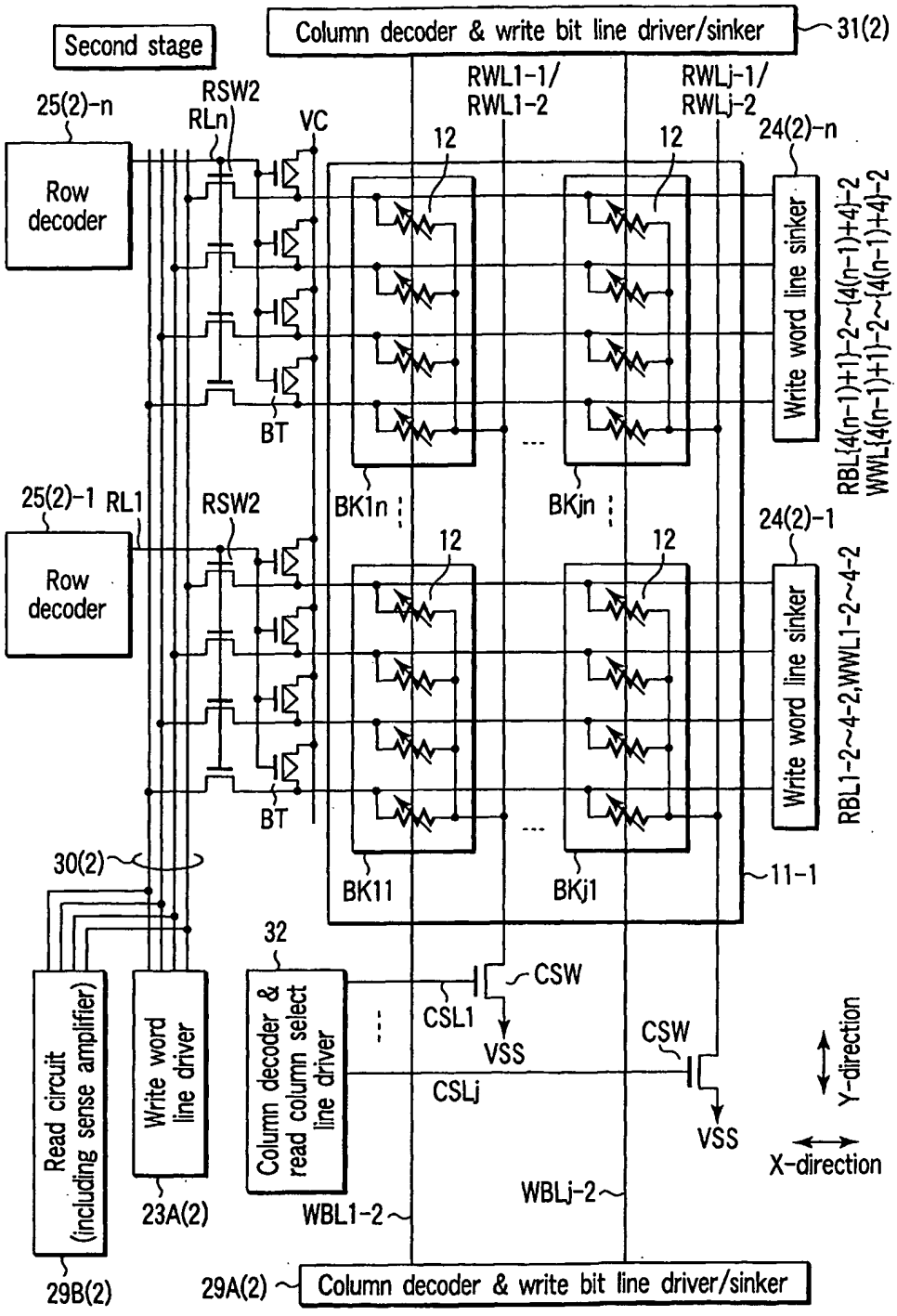
Second stage
Column decoder & write bit line driver/sinker
31(2)
25(2)-n
RSW2
RLn
VC
RWL1-1/
RWL1-2
RWLj-1/
RWLj-2
12
24(2)-n
Row decoder
Write word line sinker
RBL{4(n-1)+1}-2~{4(n-1)+4}-2
WWL{4(n-1)+1}-2~{4(n-1)+4}-2
BT
25(2)-1
RL1
RSW2
BK1n
BKjn
24(2)-1
Row decoder
Write word line sinker
RBL1-2~4-2,WWL1-2~4-2
BT
30(2)
BK11
BKj1
11-1
32
CSW
CSL1
VSS
CSW
CSLj
VSS
Y-direction
X-direction
Read circuit (including sense amplifier)
Write word line driver
Column decoder & read column select line driver
23A(2)
WBL1-2
WBLj-2
29B(2)
29A(2)
Column decoder & write bit line driver/sinker

FIG. 119

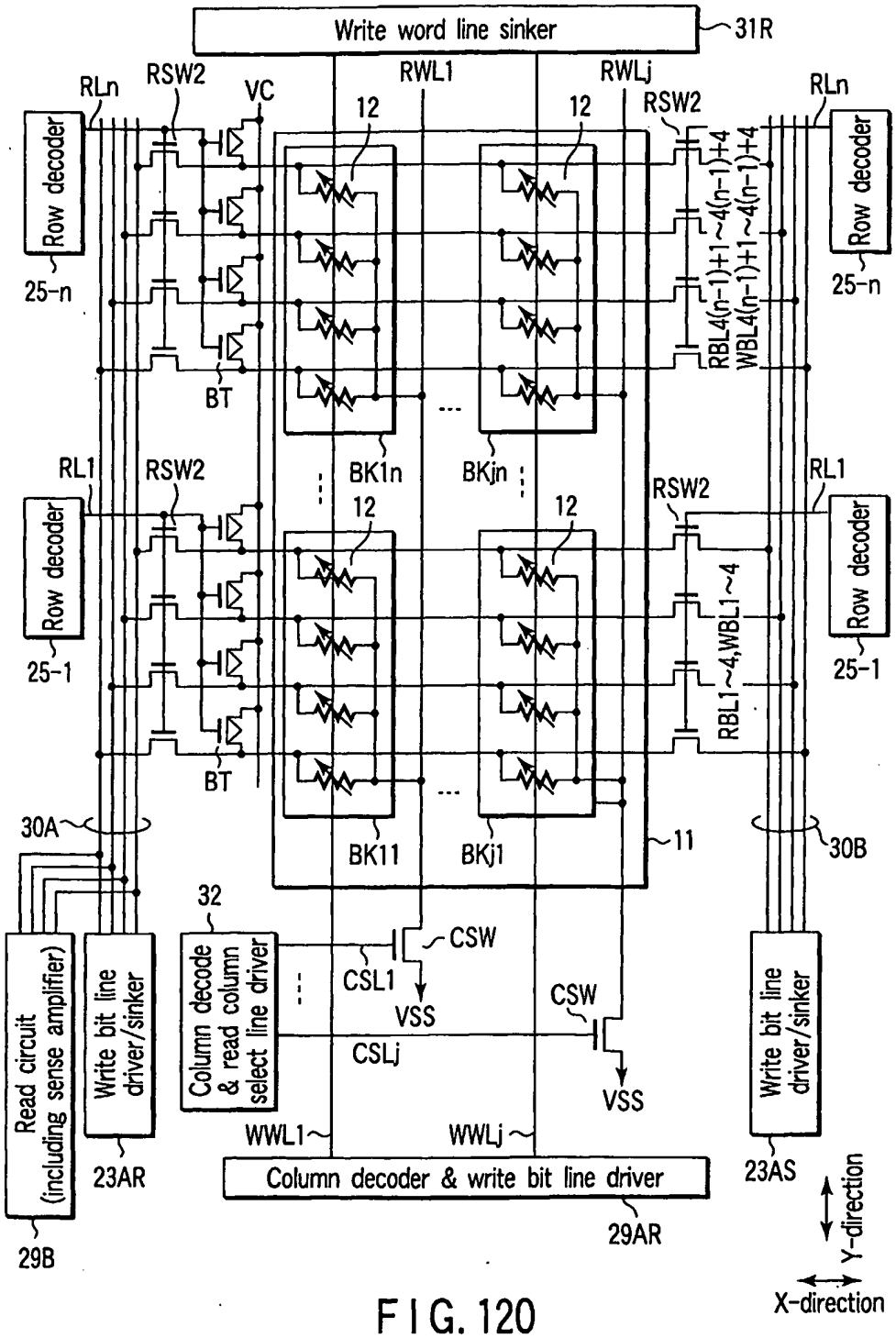
Write word line sinker
31R
RLn
RSW2
VC
RWL1
RWLj
12
Row decoder
25-n
BT
BK1n
BKjn
RBL4(n-1)+1~4(n-1)+4
WBL4(n-1)+1~4(n-1)+4
RL1
25-1
RBL1~4,WBL1~4
30A
30B
BK11
BKj1
11
32
Column decode & read column select line driver
CSW
CSL1
VSS
CSLj
Read circuit (including sense amplifier)
Write bit line driver/sinker
23AR
23AS
29B
WWL1
WWLj
Column decoder & write bit line driver
29AR
Y-direction
X-direction

FIG. 120

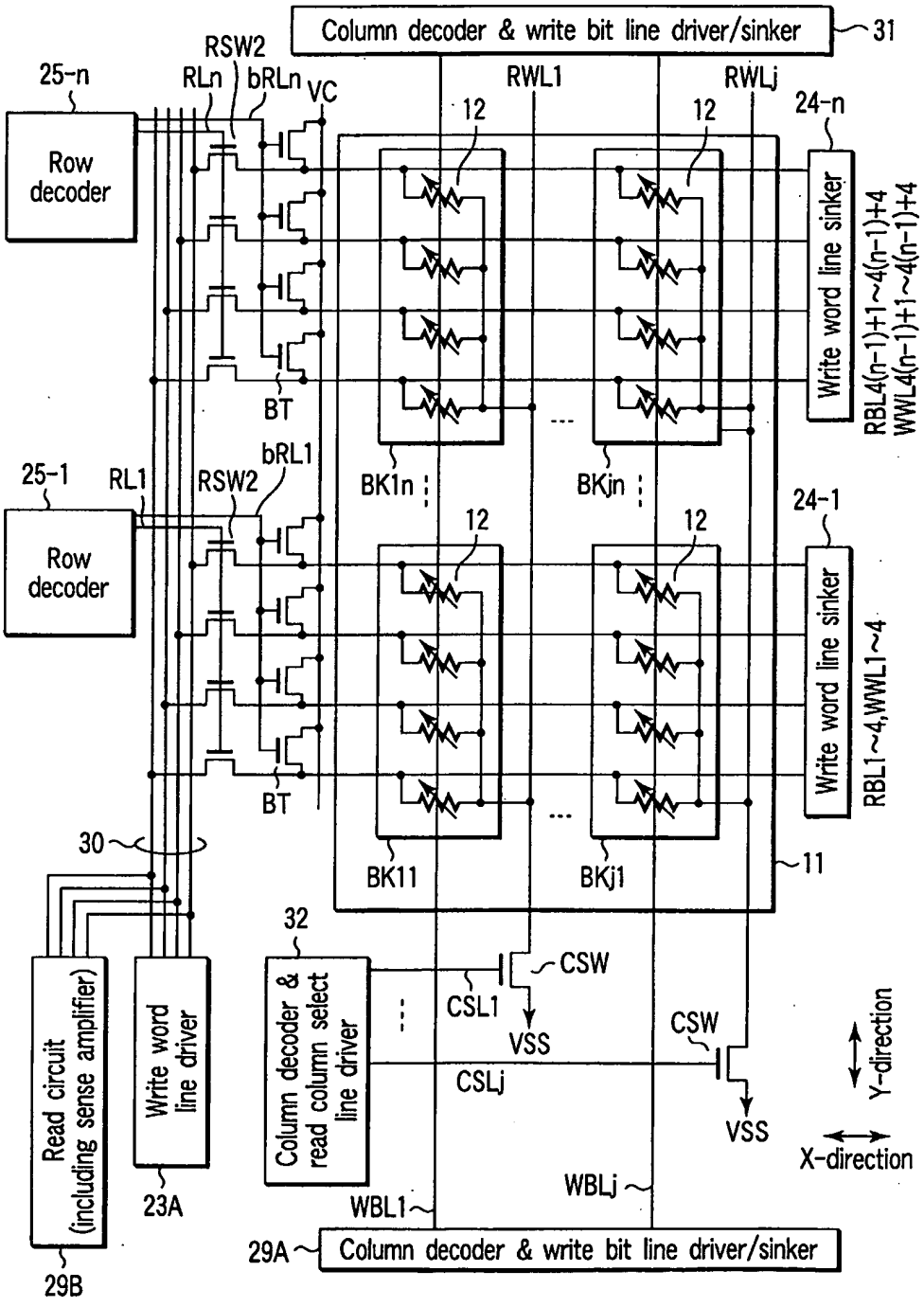
Column decoder & write bit line driver/sinker
31
RSW2
25-n
RLn
bRLn
VC
RWL1
RWLj
12
24-n
Row decoder
Write word line sinker
RBL4(n-1)+1~4(n-1)+4
WWL4(n-1)+1~4(n-1)+4
BT
bRL1
25-1
RL1
RSW2
BK1n
BKjn
24-1
Row decoder
Write word line sinker
RBL1~4,WWL1~4
BT
30
BK11
BKj1
11
32
CSW
CSL1
VSS
CSW
CSLj
VSS
Y-direction
X-direction
Read circuit (including sense amplifier)
Write word line driver
Column decoder & read column select line driver
23A
WBL1
WBLj
29A
Column decoder & write bit line driver/sinker
29B

FIG. 121

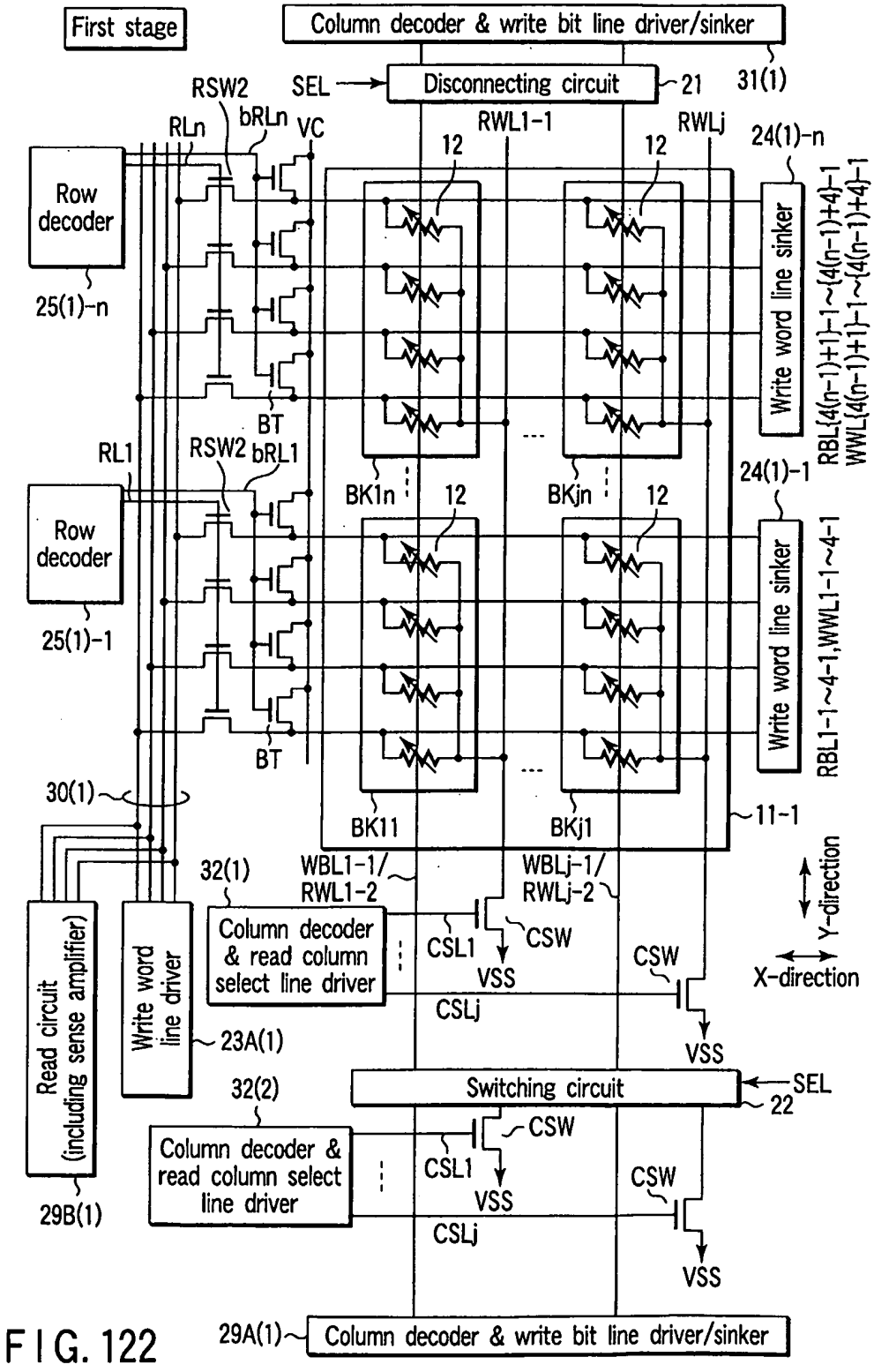
First stage
Column decoder & write bit line driver/sinker
31(1)
Disconnecting circuit
21
SEL
RSW2
bRLn
RLn
VC
RWL1-1
RWLj
12
24(1)-n
Row decoder
25(1)-n
Write word line sinker
RBL[4(n-1)+1]-1~{4(n-1)+4}-1
WWL[4(n-1)+1]-1~{4(n-1)+4}-1
BT
RL1
RSW2
bRL1
BK1n
BKjn
24(1)-1
Row decoder
25(1)-1
Write word line sinker
RBL1-1~4-1,WWL1-1~4-1
30(1)
BK11
BKj1
11-1
32(1)
WBL1-1/
RWL1-2
WBLj-1/
RWLj-2
Column decoder & read column select line driver
CSL1
CSW
VSS
CSLj
Y-direction
X-direction
Read circuit (including sense amplifier)
Write word line driver
23A(1)
32(2)
Switching circuit
SEL
22
Column decoder & read column select line driver
29B(1)
29A(1)
Column decoder & write bit line driver/sinker

FIG. 122

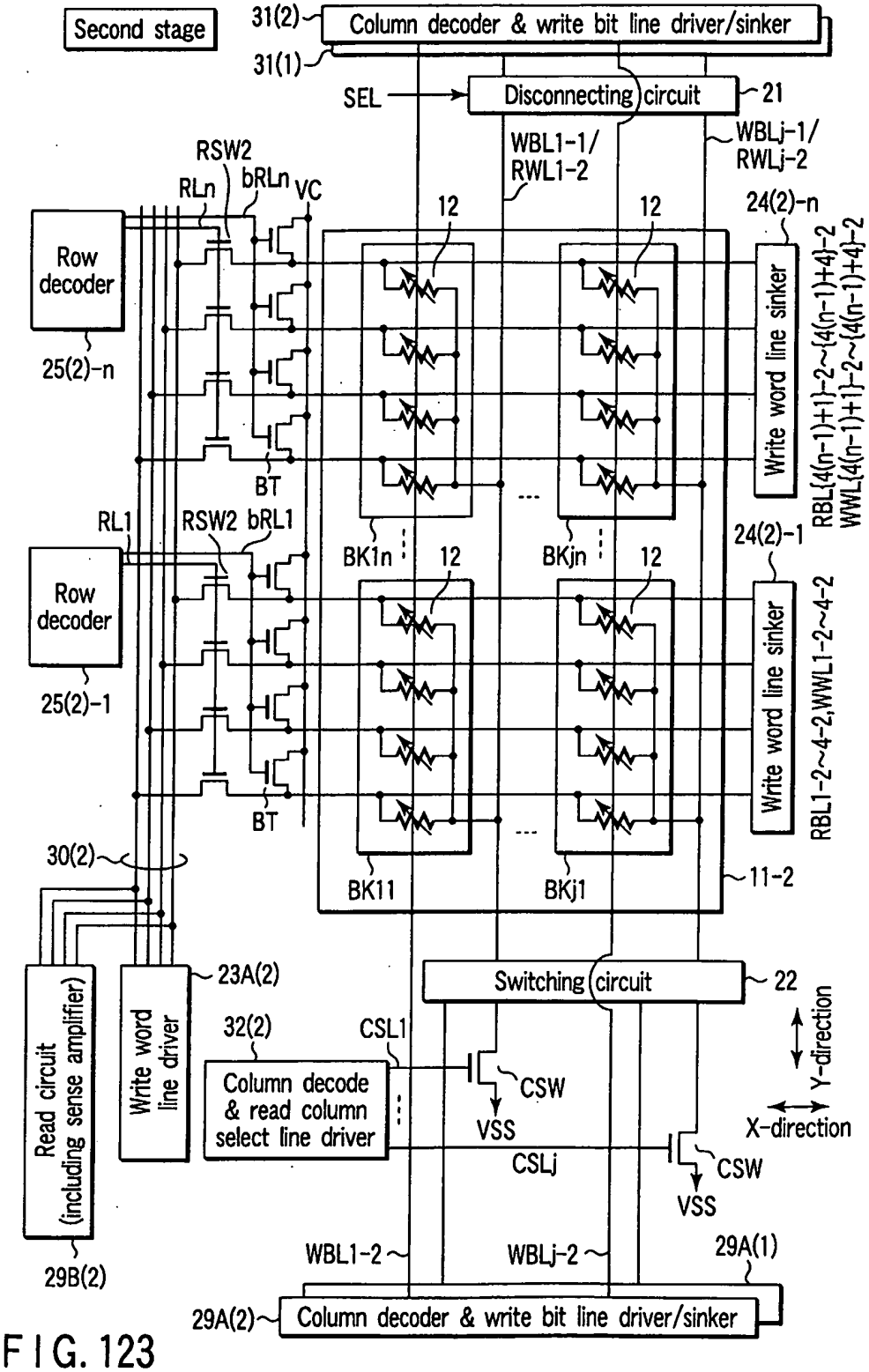
Second stage
31(2)
Column decoder & write bit line driver/sinker
31(1)
SEL
Disconnecting circuit
21
WBL1-1/
RWL1-2
WBLj-1/
RWLj-2
RSW2
RLn
bRLn
VC
12
24(2)-n
Row decoder
25(2)-n
Write word line sinker
RBL{4(n-1)+1}-2~{4(n-1)+4}-2
WWL{4(n-1)+1}-2~{4(n-1)+4}-2
BT
RL1
RSW2
bRL1
BK1n
BKjn
24(2)-1
Row decoder
25(2)-1
RBL1-2~4-2,WWL1-2~4-2
30(2)
BK11
BKj1
11-2
Switching circuit
22
23A(2)
32(2)
CSL1
CSW
Y-direction
X-direction
Read circuit (including sense amplifier)
Write word line driver
Column decode & read column select line driver
VSS
CSLj
29B(2)
WBL1-2
WBLj-2
29A(1)
29A(2)
Column decoder & write bit line driver/sinker

FIG. 123

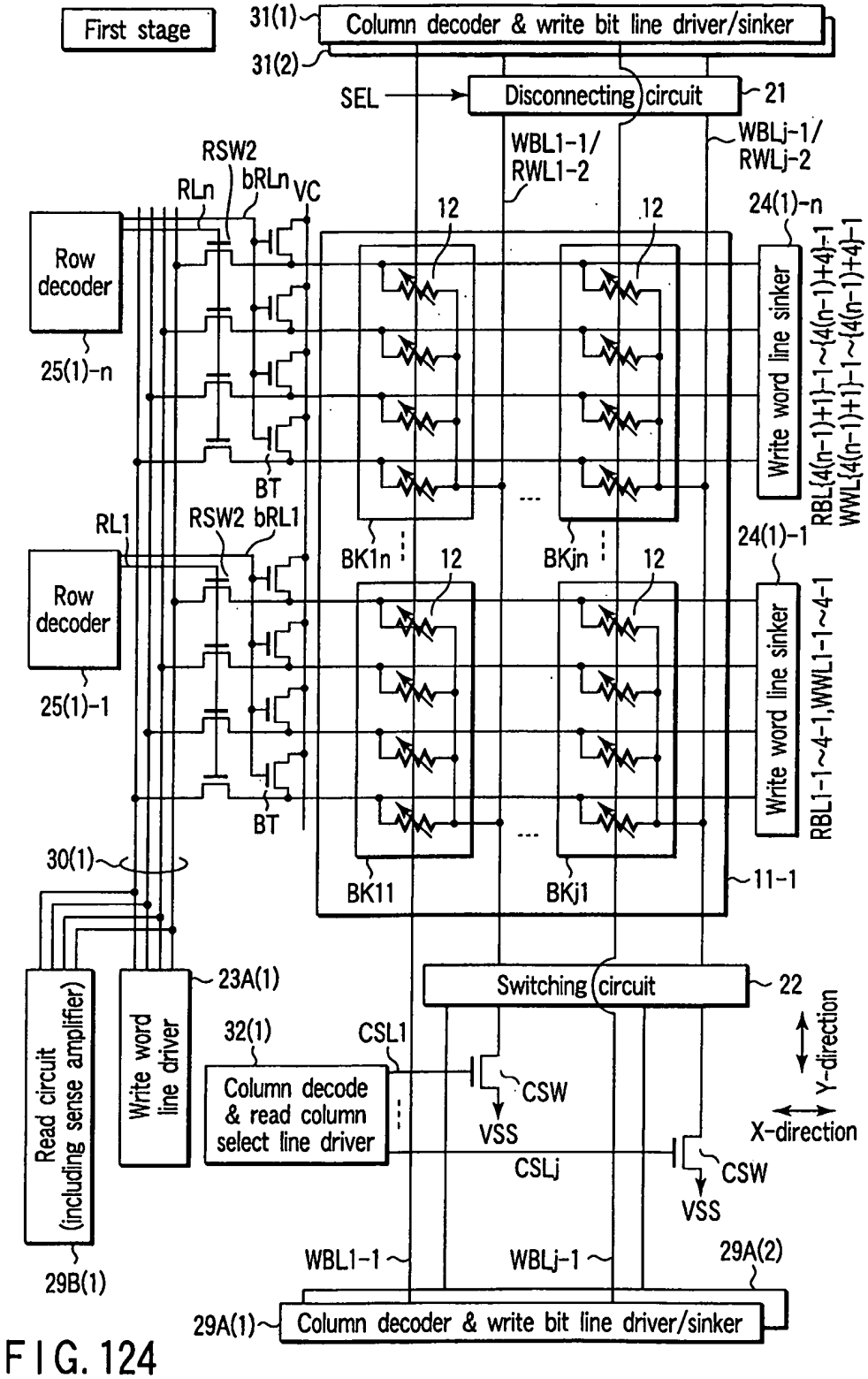
First stage
31(1)
Column decoder & write bit line driver/sinker
31(2)
SEL
Disconnecting circuit
21
WBL1-1/
RWL1-2
WBLj-1/
RWLj-2
RSW2
RLn
bRLn
VC
12
24(1)-n
Row decoder
25(1)-n
Write word line sinker
RBL{4(n-1)+1}-1~{4(n-1)+4}-1
WWL{4(n-1)+1}-1~{4(n-1)+4}-1
BT
RL1
RSW2
bRL1
BK1n
BKjn
24(1)-1
Row decoder
25(1)-1
RBL1-1~4-1,WWL1-1~4-1
30(1)
BK11
BKj1
11-1
Switching circuit
22
23A(1)
32(1)
CSL1
Read circuit (including sense amplifier)
Write word line driver
Column decode & read column select line driver
CSW
VSS
CSLj
Y-direction
X-direction
29B(1)
WBL1-1
WBLj-1
29A(2)
29A(1)
Column decoder & write bit line driver/sinker

FIG. 124

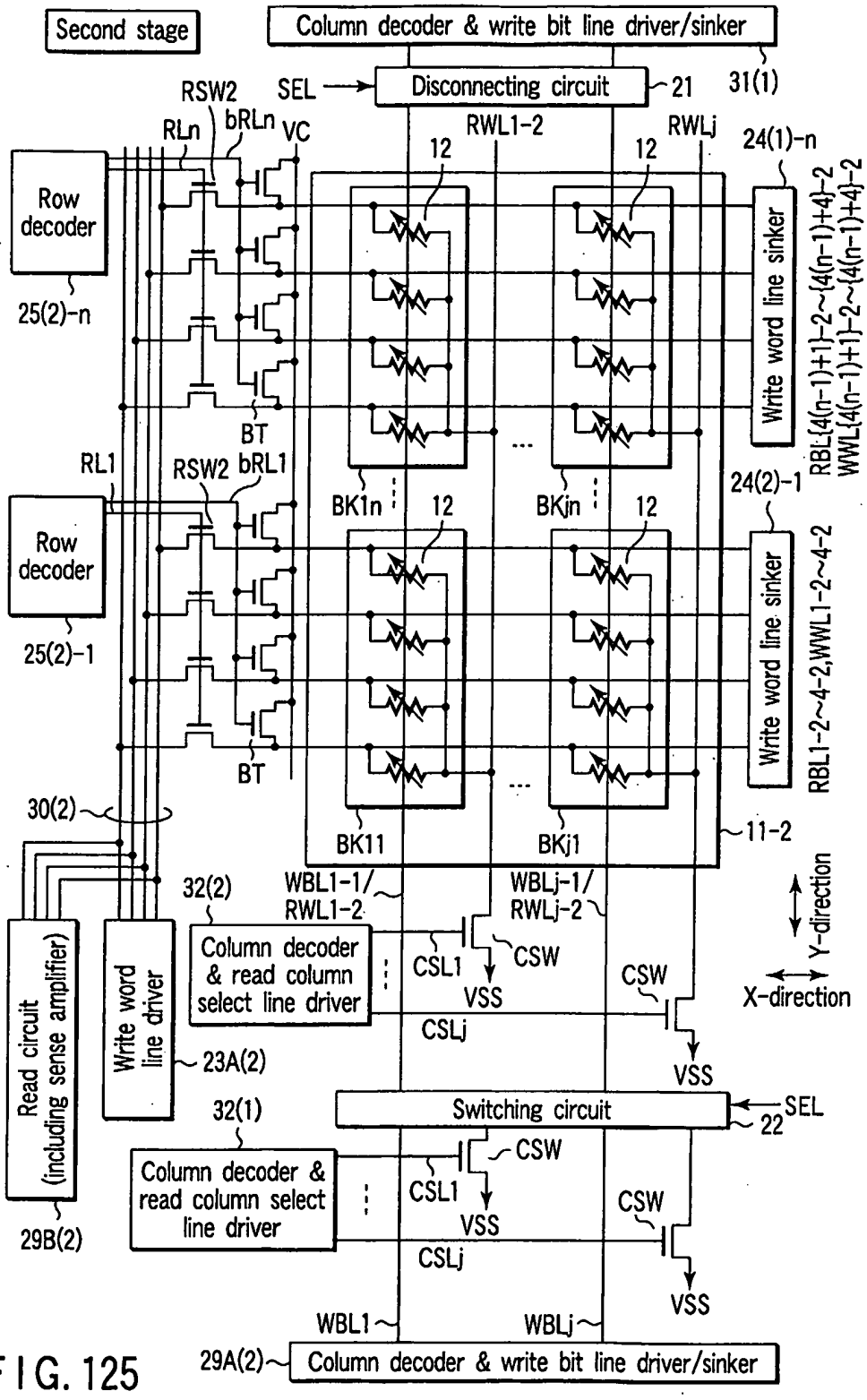
Second stage
Column decoder & write bit line driver/sinker
31(1)
SEL
Disconnecting circuit
21
RSW2
RLn
bRLn
VC
RWL1-2
RWLj
12
24(1)-n
Write word line sinker
RBL{4(n-1)+1}-2~{4(n-1)+4}-2
WWL{4(n-1)+1}-2~{4(n-1)+4}-2
Row decoder
25(2)-n
BT
RL1
RSW2
bRL1
BK1n
BKjn
24(2)-1
RBL1-2~4-2,WWL1-2~4-2
25(2)-1
30(2)
BK11
BKj1
11-2
32(2)
WBL1-1/
RWL1-2
WBLj-1/
RWLj-2
Y-direction
X-direction
Read circuit (including sense amplifier)
Write word line driver
Column decoder & read column select line driver
CSL1
CSW
VSS
CSLj
23A(2)
Switching circuit
22
SEL
32(1)
Column decoder & read column select line driver
29B(2)
WBL1
WBLj
29A(2)
Column decoder & write bit line driver/sinker

FIG. 125

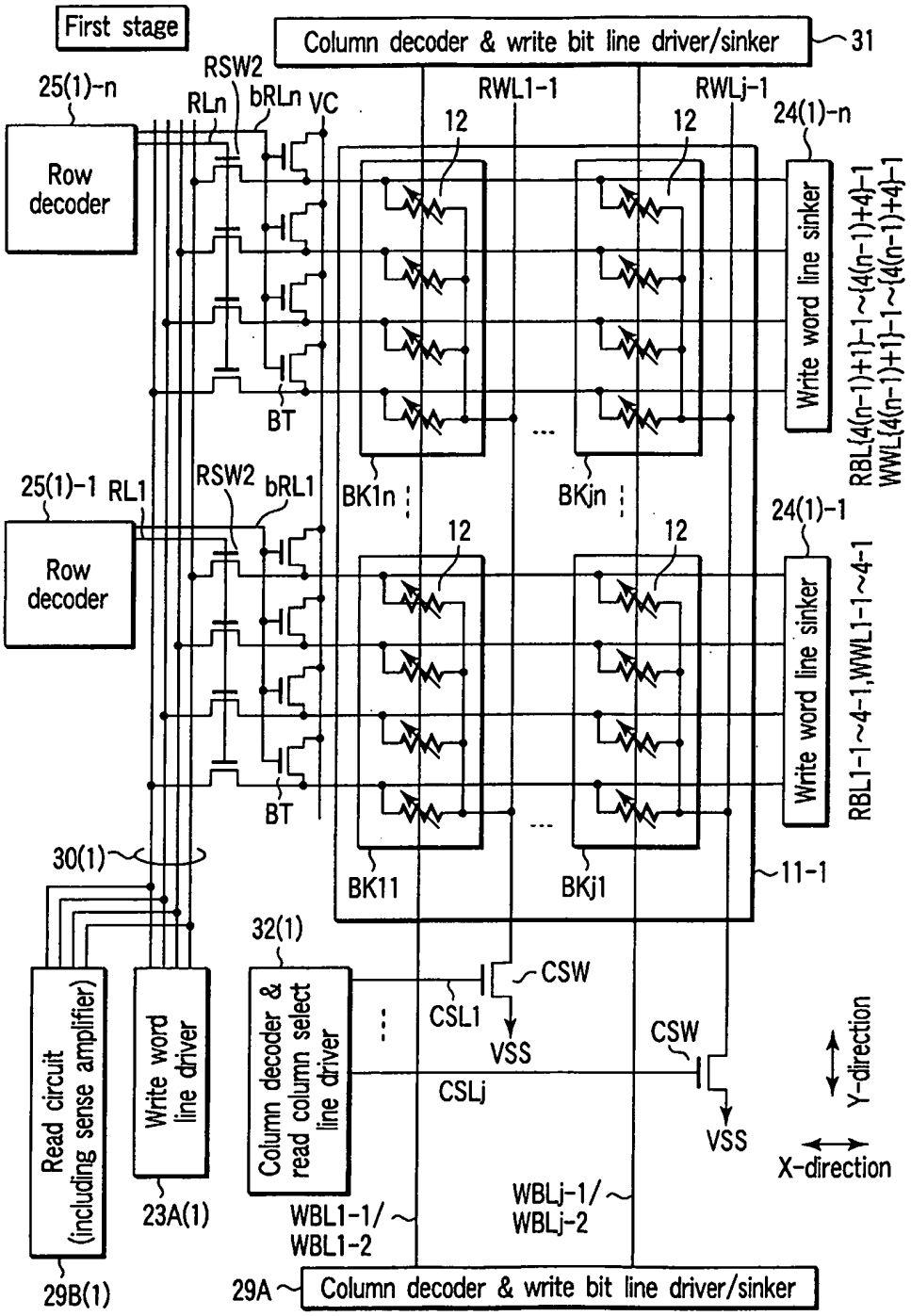
First stage
Column decoder & write bit line driver/sinker
31
25(1)-n
RSW2
RLn
bRLn
VC
RWL1-1
RWLj-1
12
24(1)-n
Row decoder
Write word line sinker
BT
BK1n
BKjn
RBL{4(n-1)+1}-1~{4(n-1)+4}-1
WWL{4(n-1)+1}-1~{4(n-1)+4}-1
25(1)-1
RL1
RSW2
bRL1
24(1)-1
RBL1-1~4-1,WWL1-1~4-1
30(1)
BK11
BKj1
11-1
32(1)
CSW
CSL1
VSS
CSLj
Y-direction
X-direction
Read circuit (including sense amplifier)
Write word line driver
Column decoder & read column select line driver
23A(1)
WBL1-1/ WBL1-2
WBLj-1/ WBLj-2
29B(1)
29A
Column decoder & write bit line driver/sinker

FIG. 126

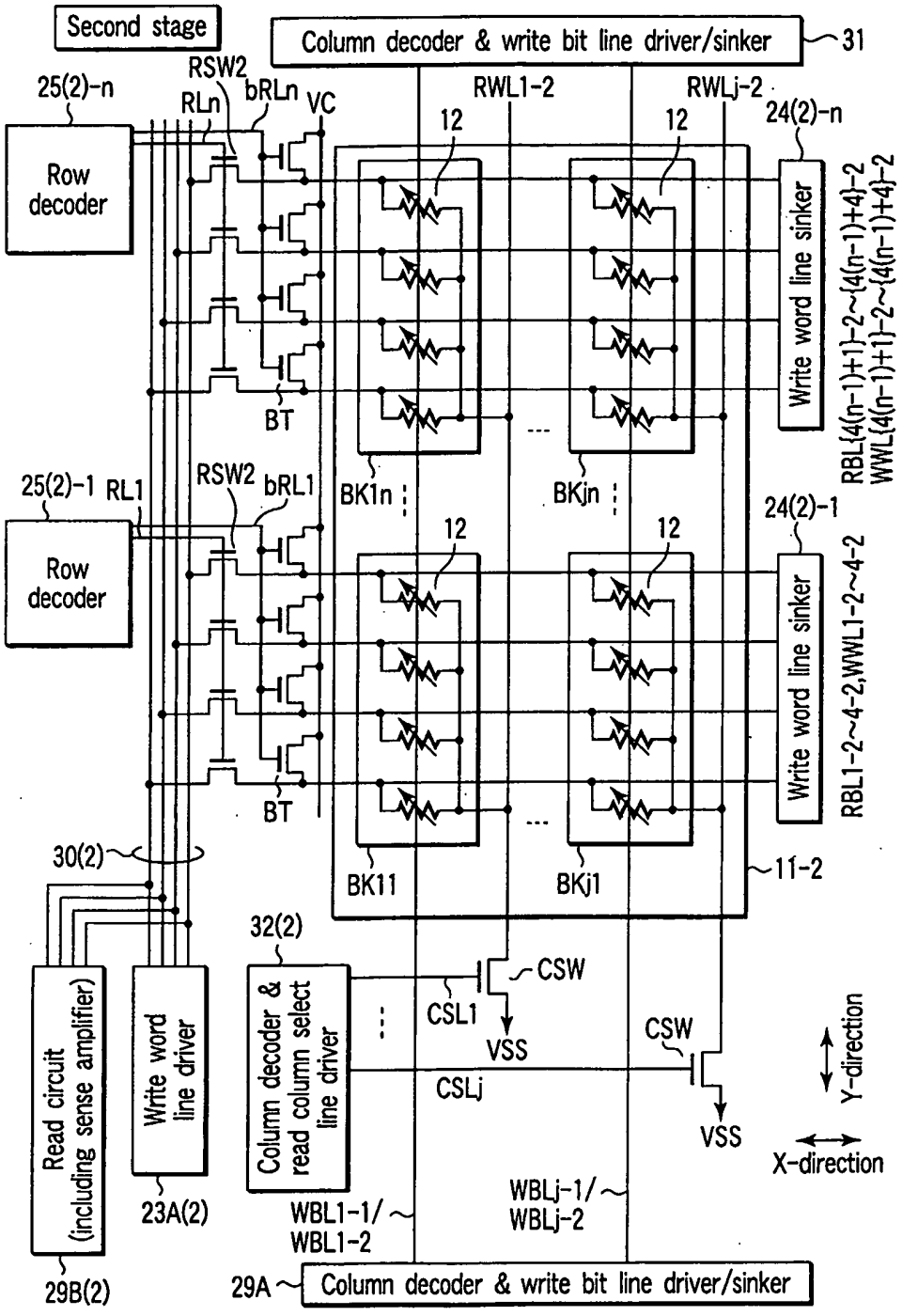
Second stage
Column decoder & write bit line driver/sinker
31
25(2)-n
RSW2
RLn
bRLn
VC
RWL1-2
RWLj-2
12
24(2)-n
Row decoder
Write word line sinker
RBL{4(n-1)+1}-2~{4(n-1)+4}-2
WWL{4(n-1)+1}-2~{4(n-1)+4}-2
BT
25(2)-1
RL1
RSW2
bRL1
BK1n
BKjn
24(2)-1
RBL1-2~4-2,WWL1-2~4-2
30(2)
BK11
BKj1
11-2
32(2)
CSW
CSL1
VSS
CSLj
Y-direction
X-direction
Read circuit (including sense amplifier)
Write word line driver
Column decoder & read column select line driver
23A(2)
WBL1-1/ WBL1-2
WBLj-1/ WBLj-2
29B(2)
29A
Column decoder & write bit line driver/sinker

FIG. 127

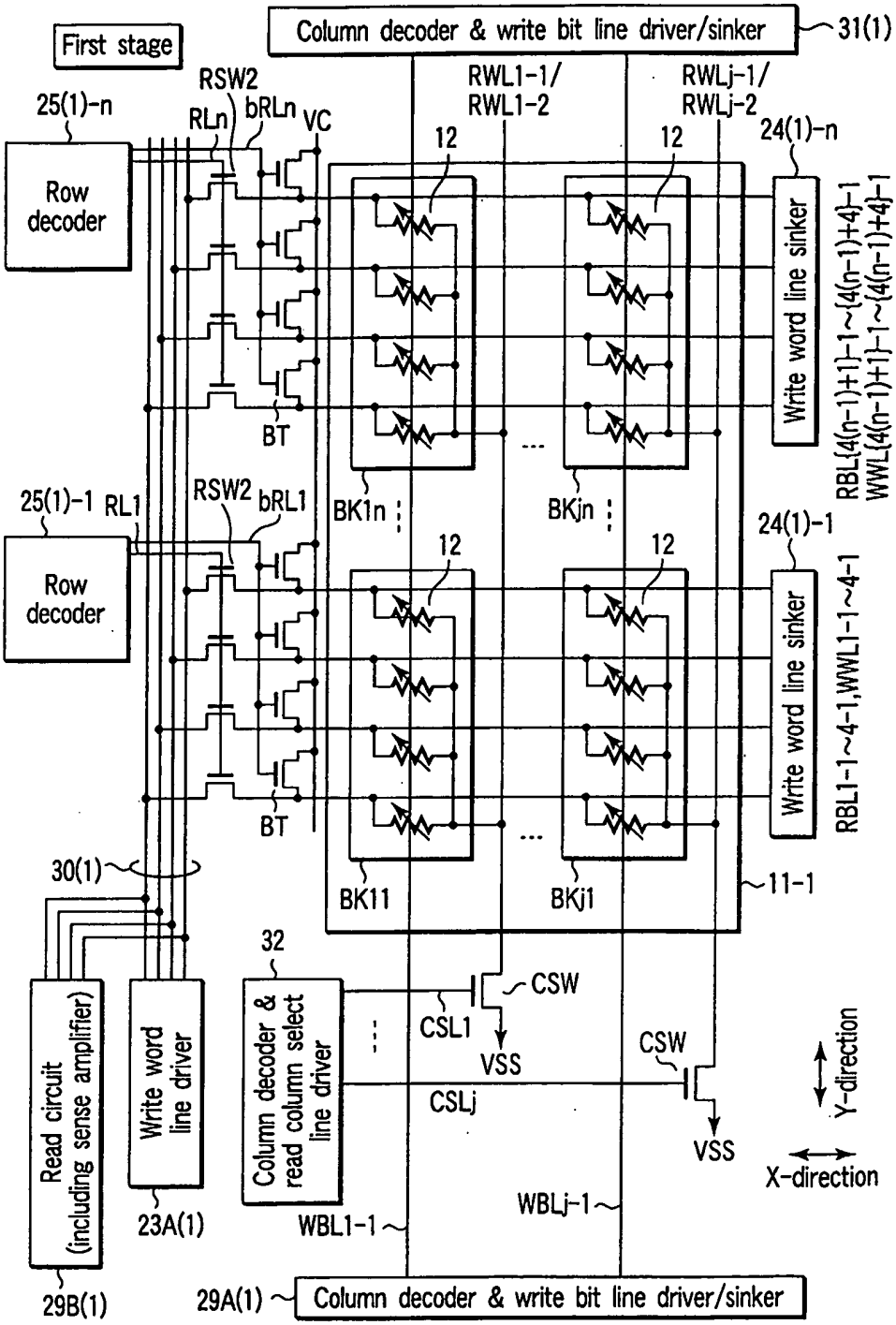
First stage
Column decoder & write bit line driver/sinker
31(1)
RSW2
RLn
bRLn
VC
RWL1-1/
RWL1-2
RWLj-1/
RWLj-2
25(1)-n
Row decoder
12
24(1)-n
Write word line sinker
RBL{4(n-1)+1}-1~{4(n-1)+4}-1
WWL{4(n-1)+1}-1~{4(n-1)+4}-1
BT
25(1)-1
RL1
RSW2
bRL1
BK1n
BKjn
Row decoder
24(1)-1
RBL1-1~4-1,WWL1-1~4-1
30(1)
BK11
BKj1
11-1
32
CSW
CSL1
VSS
CSLj
Read circuit (including sense amplifier)
Write word line driver
Column decoder & read column select line driver
23A(1)
WBL1-1
WBLj-1
Y-direction
X-direction
29B(1)
29A(1)
Column decoder & write bit line driver/sinker

FIG. 128

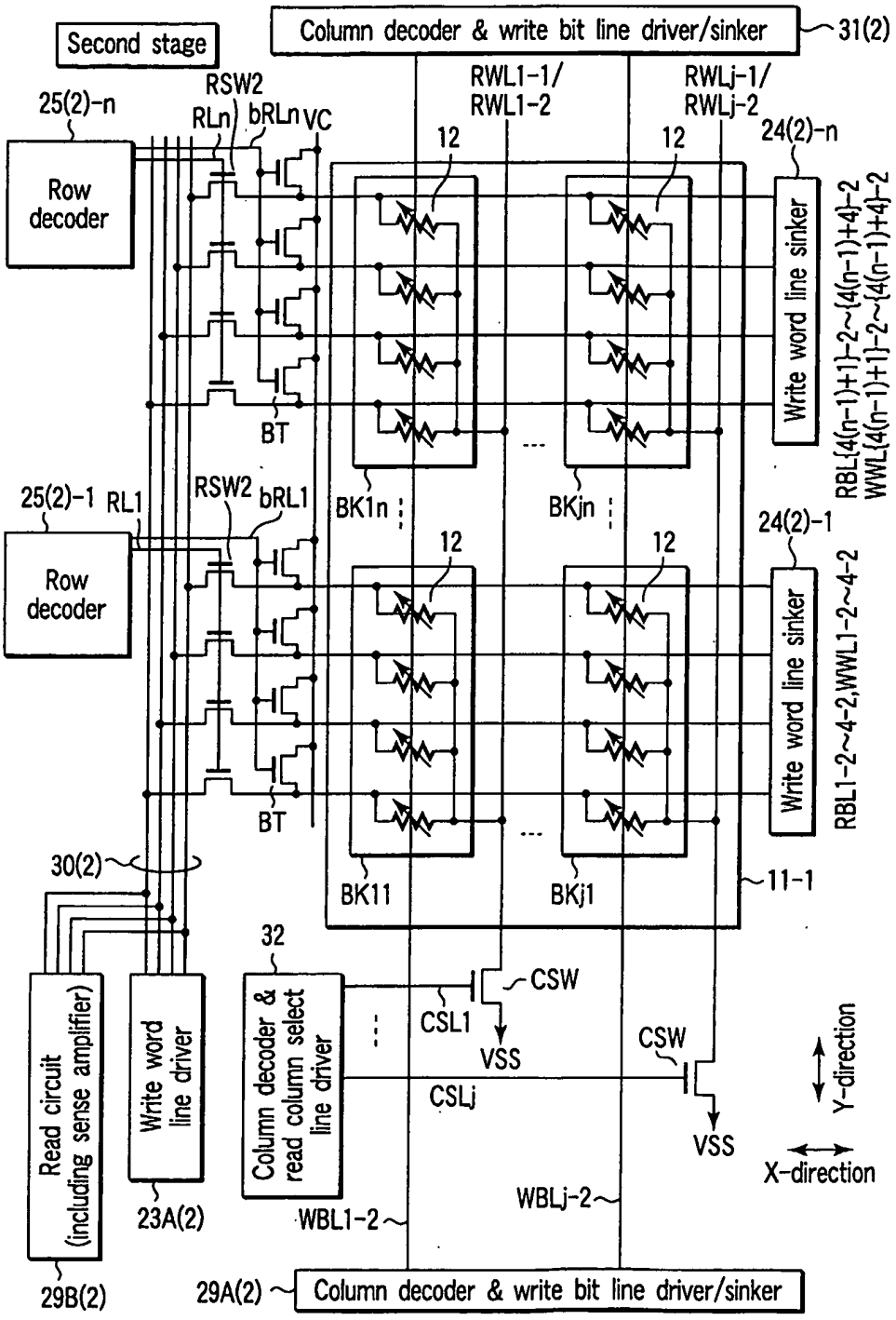
Second stage
Column decoder & write bit line driver/sinker
31(2)
25(2)-n
RSW2
RLn
bRLn
VC
RWL1-1/
RWL1-2
RWLj-1/
RWLj-2
12
24(2)-n
Row decoder
Write word line sinker
RBL{4(n-1)+1}-2~{4(n-1)+4}-2
WWL{4(n-1)+1}-2~{4(n-1)+4}-2
BT
BK1n
BKjn
25(2)-1
RL1
RSW2
bRL1
24(2)-1
RBL1-2~4-2,WWL1-2~4-2
30(2)
BK11
BKj1
11-1
32
CSW
CSL1
VSS
CSLj
Y-direction
X-direction
Read circuit (including sense amplifier)
Write word line driver
Column decoder & read column select line driver
23A(2)
WBL1-2
WBLj-2
29B(2)
29A(2)
Column decoder & write bit line driver/sinker

FIG. 129

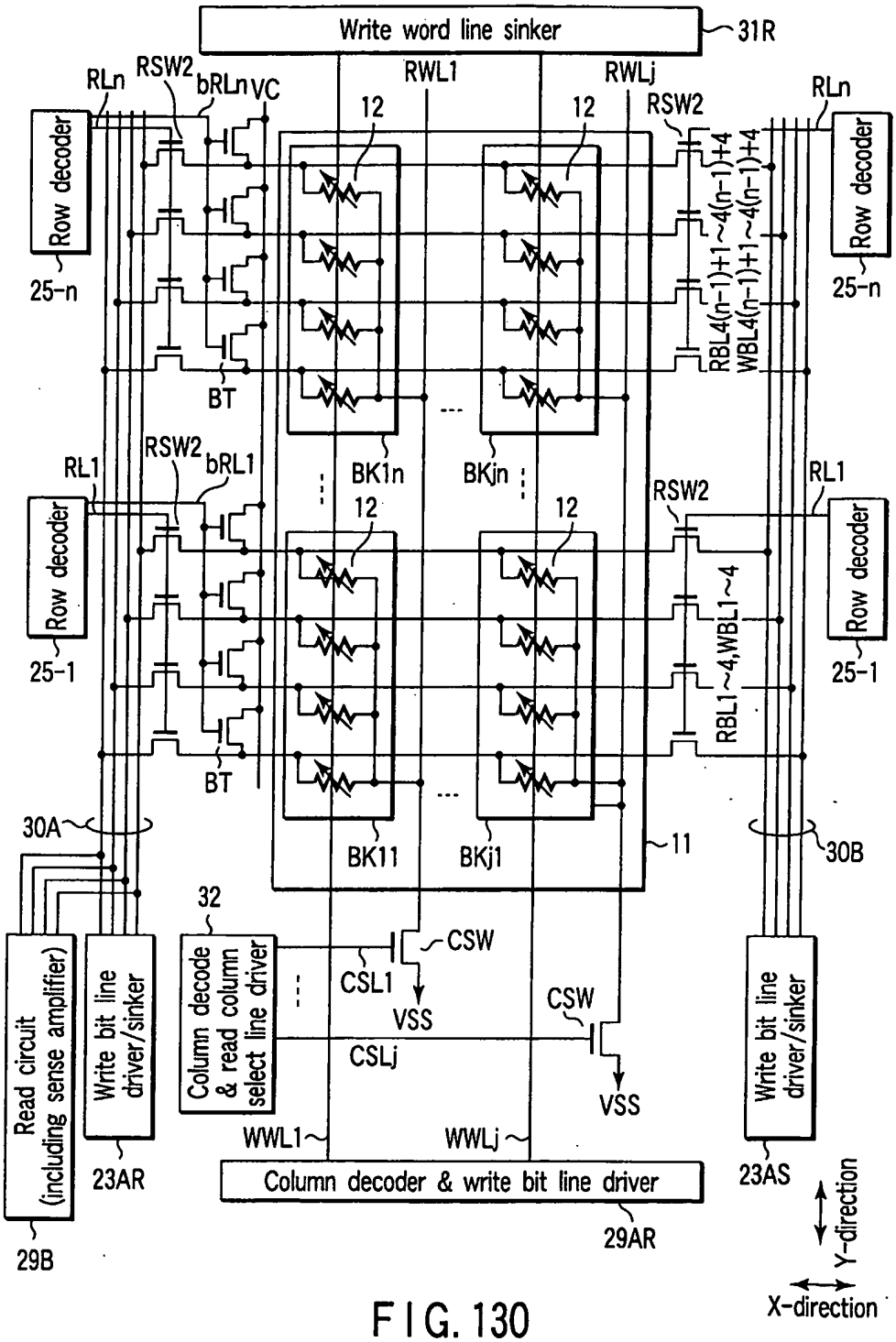
Write word line sinker
31R
RLn
RSW2
bRLn
VC
RWL1
RWLj
12
Row decoder
25-n
BT
RBL4(n-1)+1~4(n-1)+4
WBL4(n-1)+1~4(n-1)+4
RL1
bRL1
BK1n
BKjn
RSW2
RBL1~4,WBL1~4
25-1
30A
30B
BK11
BKj1
11
32
Column decode & read column select line driver
CSW
CSL1
VSS
CSLj
Read circuit (including sense amplifier)
Write bit line driver/sinker
23AR
23AS
WWL1
WWLj
Column decoder & write bit line driver
29AR
29B
Y-direction
X-direction

FIG. 130

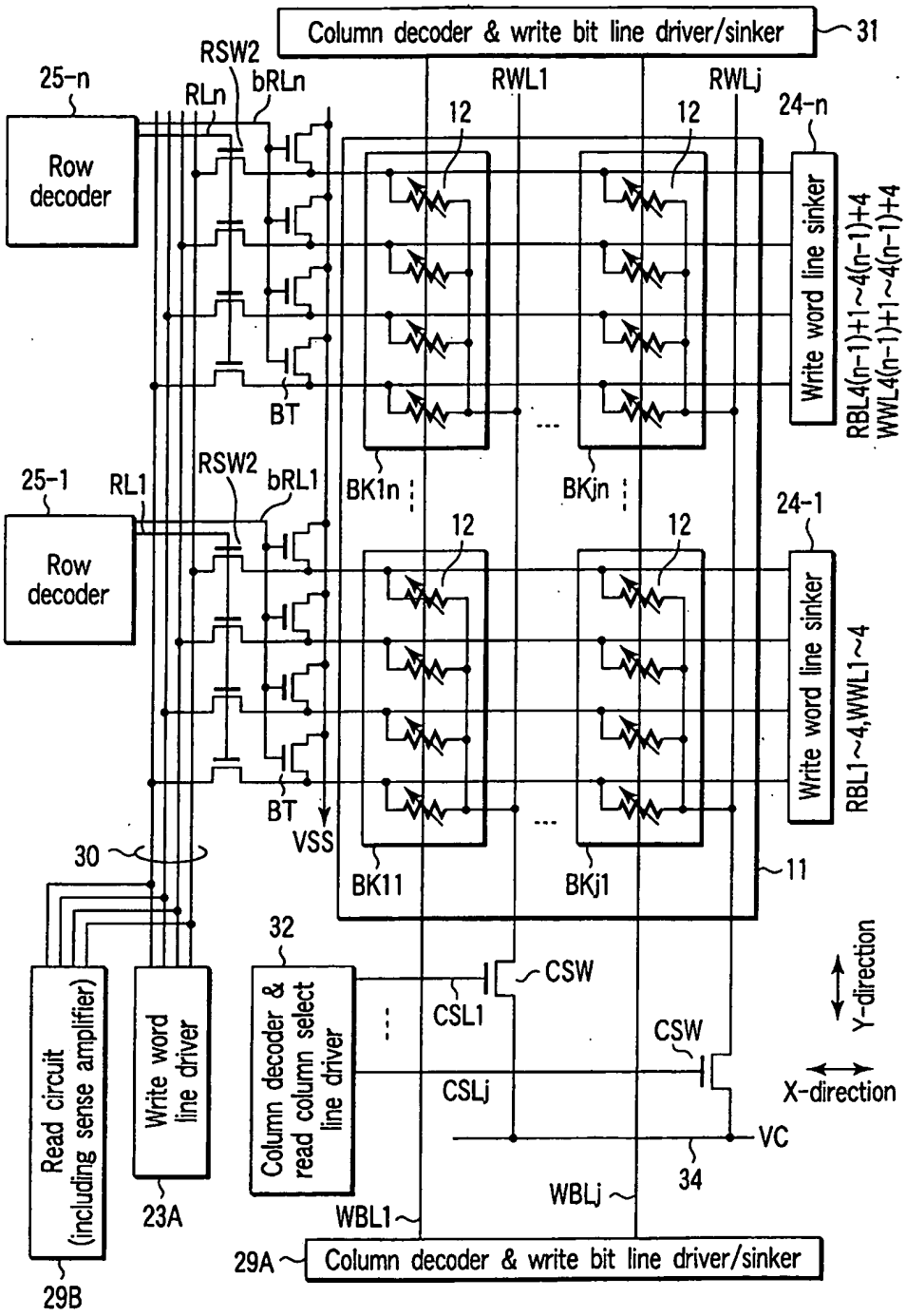
Column decoder & write bit line driver/sinker
31
RSW2
25-n
RLn
bRLn
RWL1
RWLj
12
24-n
Row decoder
Write word line sinker
RBL4(n-1)+1~4(n-1)+4
WWL4(n-1)+1~4(n-1)+4
BT
25-1
RL1
RSW2
bRL1
BK1n
BKjn
24-1
Row decoder
Write word line sinker
RBL1~4,WWL1~4
BT
VSS
30
BK11
BKj1
11
32
CSW
Read circuit (including sense amplifier)
Write word line driver
Column decoder & read column select line driver
CSL1
CSW
Y-direction
CSLj
X-direction
VC
34
WBLj
WBL1
23A
29A
Column decoder & write bit line driver/sinker
29B

FIG. 131

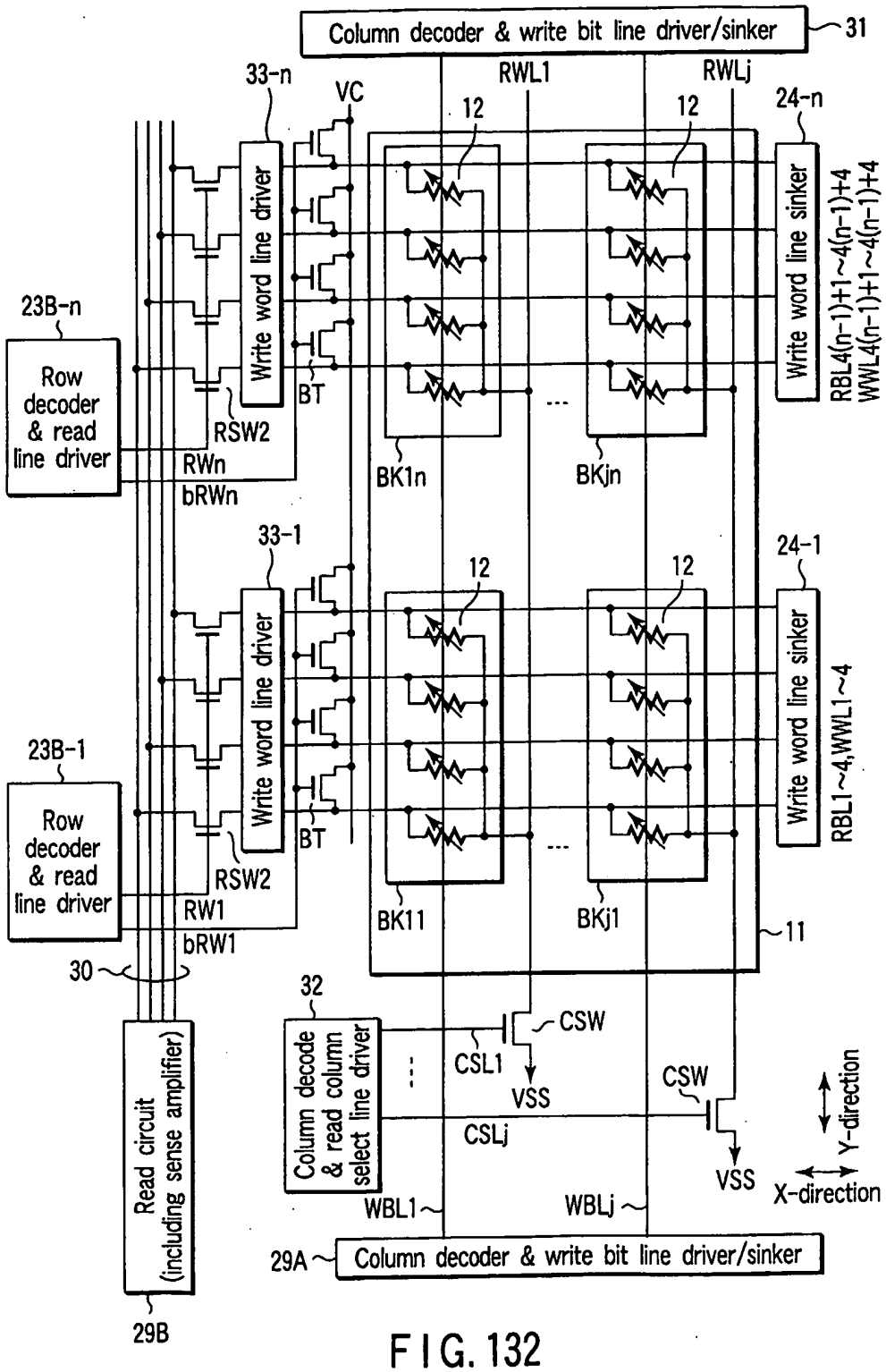
Column decoder & write bit line driver/sinker
31
33-n
VC
RWL1
RWLj
12
24-n
Write word line driver
Write word line sinker
RBL4(n-1)+1~4(n-1)+4
WWL4(n-1)+1~4(n-1)+4
23B-n
Row decoder & read line driver
BT
RSW2
RWn
bRWn
BK1n
BKjn
33-1
24-1
23B-1
RBL1~4,WWL1~4
RW1
bRW1
BK11
BKj1
11
30
32
Column decode & read column select line driver
CSW
CSL1
VSS
CSLj
Y-direction
X-direction
Read circuit (including sense amplifier)
WBL1
WBLj
29A
29B

FIG. 132